

# Considerations about Gaintracking and EMI in a VLSI Mixed Signal BiCMOS Design - A Case Study

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## ABSTRACT

Switching noise is an increasingly serious concern in the design of mixed-signal integrated circuits. This paper describes the influence of signal correlated transients produced in the digital part of a CODEC chip and measures to improve the insensitivity of the analog part. Additionally, the circuit behaviour in case of electromagnetic interference will be discussed.

## I. INTRODUCTION

The scaling of VLSI technologies opens the possibility to realize complete systems that integrate complex, digital circuits together with high-performance analog circuits. An example for such a mixed signal design is the SLICOFI<sup>®</sup>, an integrated one chip Subscriber Line Interface and CODEC Filter. A block diagram and a detailed description of this chip is given elsewhere [1]. The digital circuits work with clock frequencies ( $f_{\text{Clock}} > 4 \text{ MHz}$ ) well above the voice band ( $f_{\text{Signal}} = 0,3...3,4 \text{ kHz}$ ) but nevertheless there is a strong influence of signal correlated noise produced in the digital part. The analog part of the chip acts like a mixer and the signal dependent interferences of the digital part are folded into the voice band. These intermodulation products are then processed together with the desired signal. The problem of intermodulation distortion is well-known and will not be discussed further here. The goal of this paper is to give a survey of measures that can be implemented in a design flow to improve the insensitivity of a mixed signal design with respect to electromagnetic interferences. Furthermore considerations about gaintracking are discussed.

## II. GAINTRACKING BY POWER BUS NOISE

In the field of telecommunication gaintracking defines the variation of gain with respect to amplitude variation [2]. In this sense, it is a measure for the linearity of a transmission path in-

cluding data conversion. One well known reason is the nonlinear transfer characteristic of A/D- or D/A-converters. Another effect, the influence of signal correlated noise on power bus lines, which degrades the gaintracking behavior especially for small signal amplitudes, will be discussed in detail. As the measured frequency spectrum at the digital power supply pin (Fig. 1) shows, the on-chip digital signal-processor (DSP) generates signal correlated components around the clock frequency. Applying a two's complement sinusoid signal to a busdriver causes similar signal modulation with the difference that the modulated components are dominated by multiples of twice the signal frequency. This effect results from the increased switching transients at zero-crossing, whereby the amplitude is nearly the same for both positive and negative zero-crossings. If the signal is modified in a way that zeros are added between the signal samples (as it is the case for precharged data buses), amplitude modulation will occur at signal frequency (Fig. 2), hence the current at positive zero-crossing is less than in the negative case. Obviously this type of disturbance will degrade the gaintracking behavior, especially if decoupling of the analog and the digital part is not sufficient. Using unsigned data representation instead of two's complement arithmetic for DSP algorithms the amplitude of the modulated components can be reduced significantly (Fig. 3), thus improving the gaintracking behavior to meet the specification even in the worst case (Fig. 4).

To prevent noise injection from the digital into the analog part, separate supply lines are used on-chip (Fig. 5). The digital supply current  $i_{DD}$  produces voltages across the bond inductors  $L_1$  and  $L_2$ , the external board impedances  $Z_{11}$  and  $Z_{21}$  and the external decoupling capacitor  $C_{B1}$ . To prevent the injection of noise into the analog part, decoupling capacitors with low intrinsic impedance should be connected directly to the chip. Furthermore, the impedances  $Z_{12}$  and  $Z_{22}$  should be maximized in order to optimize the decoupling between the analog and the digital circuitry [3]. Under these circumstances, the gaintracking could be improved, even without the implementation of unsigned data representation for digital signal processing.

Anyway, the measurements showed that on-chip coupling effects, considered by the impedance  $Z_C$  in Fig. 5, can be neglected.

### III. EFFECTS OF RF INTERFERENCES

In typical applications, the SLICOFI<sup>®</sup> must tolerate large high frequency interfering signals emanating from an external source, which can cause significant interference problems. The measurement in Fig. 6 (curve a) shows the demodulated voltage in the voice band at the analog output under the influence of an electromagnetic field with an intensity of 3 V/m and frequencies between 220 MHz and 1 GHz (80 percent amplitude modulated by an 1 kHz signal). The RF signal is received by an antenna structure on the board and demodulated by the analog circuits. It indicates a wide range of sensitivity.

### IV. MEASURES TO IMPROVE THE EMC/EMI INSENSITIVITY – AN EXAMPLE

The best approach to low-distortion design is to address each distortion source separately. Therefore, the analog part was investigated by time domain simulations. Two error voltages with frequencies of 16 and 16,001 MHz were connected in series to  $V_{DD}$ ,  $V_{SS}$  or to analog ground. The

intermodulation products at the output were investigated. It could be proved by simulations and additionally by measurements, that only the nonlinearity of the output amplifiers is responsible for the demodulation of the signal correlated noise. The simulation results of the folded-cascode amplifier in Fig. 7 will be considered briefly here:

- Interferences on the positive supply voltage  $V_{DD}$  are folded by the diodes  $D_1..D_3$  used for biasing the cascode transistors  $T_{1,2}$  and the transistors  $T_{3,4}$  of the common mode circuit;
- Interferences on the negative supply voltage  $V_{SS}$  are folded by the transistors  $T_{5,6}$  of the differential input stage of the common mode circuit;
- As well interferences on ground are folded by this differential input stage;
- Interferences on the reference voltages  $V_P$  and  $V_N$  of the central bias block are folded by the current mirror transistors.

After implementation of RF decoupling measures, characterized by dashed lines in Fig. 7, the insensitivity of the amplifier could be improved considerably. The essential reason for the sensitivity peak in Fig. 6 (curve a) is the resonant circuit at the base node of transistor  $T_6$ , which consists of the on-chip capacitance at this bondpad, the bond inductance  $L_{cm}$  and the external capacitor  $C_{Ext}$ . By introducing a small resistor of  $100 \Omega$  in series to  $C_{Ext}$  the damping ratio of this antenna structure can be increased and therefore the demodulated voltage can be significantly decreased (curve b in Fig. 6).

## V. SUMMARY

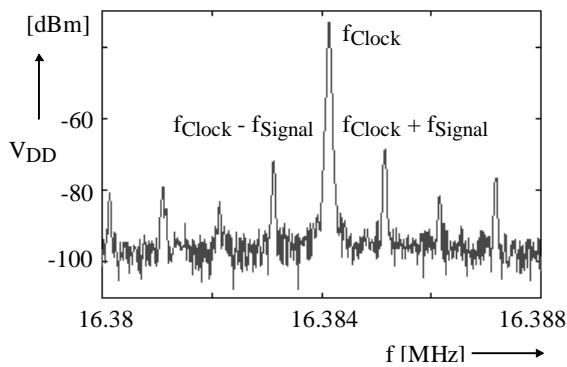
We discussed several steps that can be adopted in the design flow in order to minimize susceptibility to injected noise. First of all, the generation of signal correlated noise in the digital part of the examined chip, which is one reason for a gain error in the transmission path, can be prevented by implementing an unsigned data representation (Quit the Talker). By optimizing the board layout we reduced the interferences (Isolate the Listener) [4]. The insensitivity of the analog circuits can be improved by the integration of decoupling measures at the “hot“ nodes (Close the Listener’s ears).

## ACKNOWLEDGEMENTS

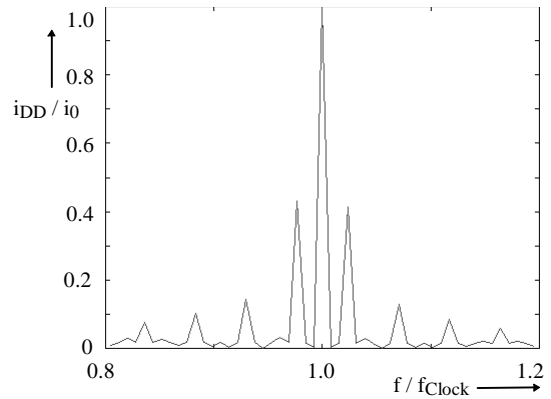
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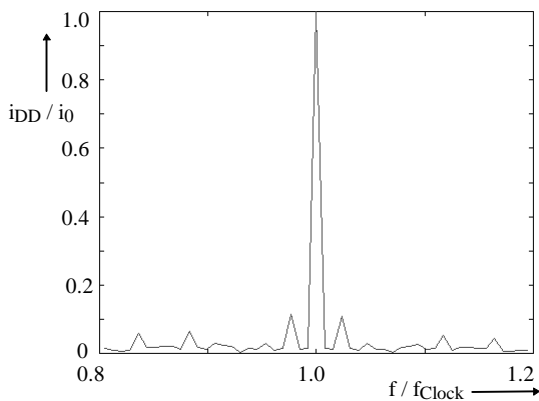
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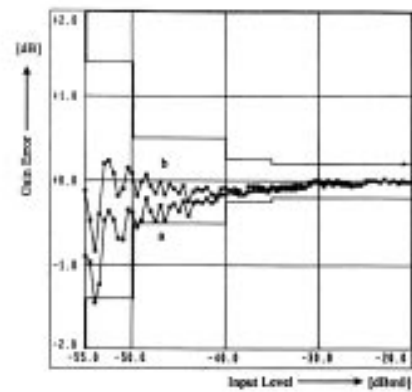
**Fig. 1** Measured spectrum of the digital supply voltage.



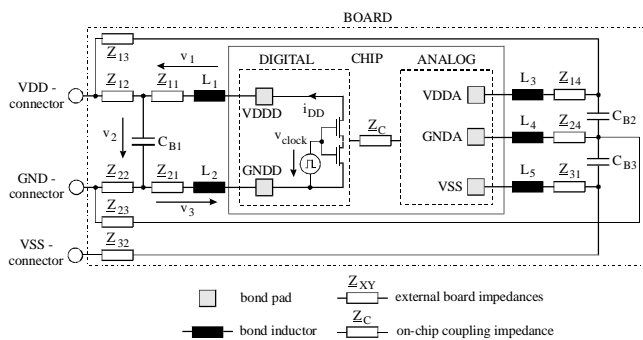
**Fig. 2** Simulated spectrum of the digital supply current with added zeros.



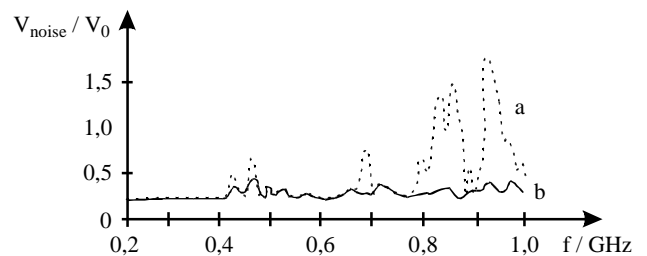
**Fig. 3** Simulated spectrum of the digital supply current for an unsigned data representation.



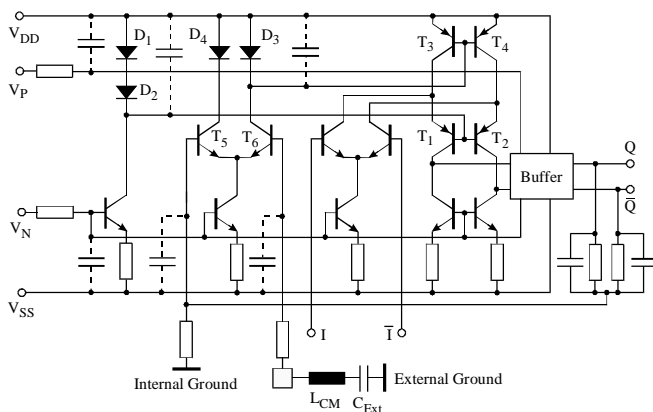
**Fig. 4** Measured gaintracking performance at 1014 Hz: a) signed data representation b) unsigned data representation.



**Fig. 5** Simplified model to describe the coupling mechanisms.



**Fig. 6** Measured intermodulation products at 1 kHz a) without damping resistor b) with damping resistor.



**Fig. 7** Folded-cascode amplifier (decoupling measures are characterized by dashed lines).