A Low-Power True Single Phase Clocked (TSPC) Full-Adder

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Abstract

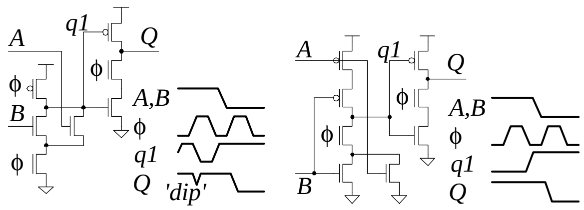
A TSPC full-adder circuit containing only 6 clock transistors and thus consuming significantly less power than recently published full-adders has been designed and characterized by simulation. It is composed of 36 transistors and consumes 220 μW @100 MHz when connected to a 5 V power supply, using a 0.8 μm standard CMOS process technology. This considers all parasitic capacitances as well as the power needed for clocking. Although minimum size transistors are used exclusively, and precharge gates are avoided in order to minimize power consumption, the operating frequency may be raised up to 290 MHz.

1 Introduction

Basic principles of low-power design are briefly recalled here, for a detailed analysis refer to [1]. Dynamic power consumption is assumed to play the dominant role within low-power CMOS circuits; it is given by

$$P_{dyn} = V_{DD}^2 \cdot f \cdot \sum C_i \cdot p_i. \tag{1}$$

Power reduction is most effectively done by lowering the supply voltage V_{DD}, however, the maximum circuit speed decreases approximately linearly with V_{DD}. Moreover, V_{DD} is often determined by system considerations, and therefore seen as a constant from the circuit designer's view. A mere reduction of the frequency f will reduce the circuit performance to the same extent as P_{dyn}. The only part of equation (1) depending on the circuit design itself is $\sum C_i \cdot p_i$. Each node capacitance C_i of a circuit is multiplied by its activity rate p_i, which describes how often signal changes occur on a specific node i. Exclusive use of minimum size transistors obviously reduces the C_i's. In addition, within a pipelined system the p_i's may be lowered by choosing an appropriate clocking technique. The next section focuses on this issue with respect to TSPC circuits. In section 3 a TSPC full-adder with minimized power consumption is presented. Finally in section 4, the effectiveness of this full-adder design is proved by comparing it with other full-adders published recently.



(a) N precharge (b) Double N-C^{2}MOS

Figure 1: TSPC *OR* latch design styles

2 Low-Power TSPC Circuits

Fig. 1 shows two possible TSPC implementations of an N clocked latch performing a logical *OR* function. Version (a) uses precharge technique, while version (b) is composed of two N-C^{2}MOS gates. For a detailed functional description refer to [2]. The precharged version consists of one transistor less and has a lower capacitive load on its inputs, which makes device scaling more effective when high speed is desired. On the other hand, device scaling is undesired in a low-power circuit as it increases the corresponding C_i's. When using minimum size transistors, routing and diffusion capacitances are in the same order of magnitude as gate capacitances, which makes the increased capacitive load on the inputs of version (b) less significant. As the clock changes twice during one cycle, its activity rate is given by $p_i = 1$. A statistical data signal changing on average only every second cycle has a four times lower activity rate $p_i = 0.25$. The output $q1$ of the precharge *NOR* of version (a) toggles between precharge and evaluate state when it is continuously evaluated, so the activity rate may be estimated with $p_i = 0.5$ for a statistical output signal. So-called dips within the signal Q of version (a) also lead to a significant increase of p_i compared to version (b). As precharge gates have one more clock transistor and a higher node activity rate, power dissipation is significantly increased especially within low fan-in gates with minimum size transistors. In particular, simulation indicates that version (b) of the TSPC *OR* latch consumes 58% less energy than version (a).

3 Low-Power Full-Adder Circuit

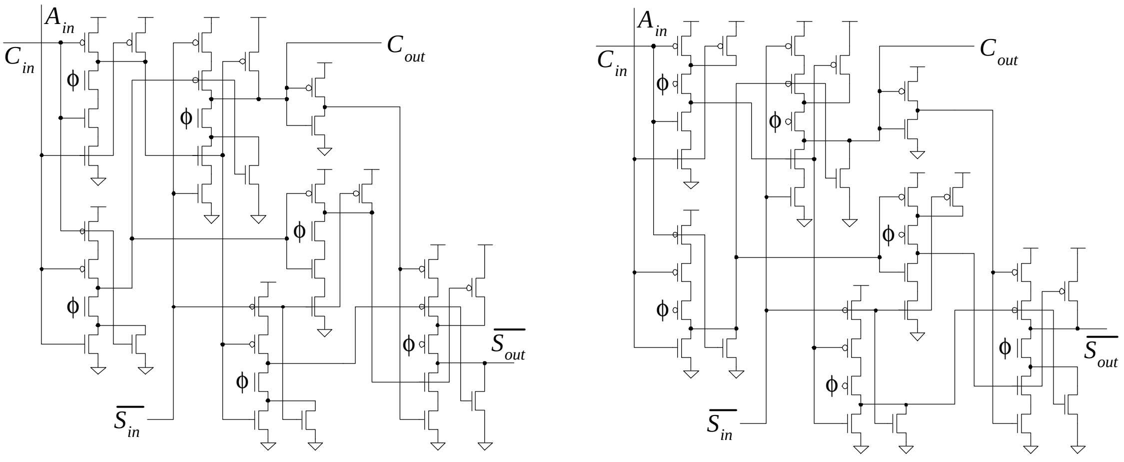
As reduced clock transistor count is intended, a half cycle full-adder design is prefered against a full cycle one. So for a TSPC implementation a N type full-adder and a P type full-adder are needed. Fig. 2 shows the transistor schematics of the N and P type full-adder circuits; their logic equivalent is given in fig. 3, which also illustrates the pipeline scheme of subsequent full-adders. The carry signal is calculated according to

$$C_{out} = (C_{in} \cdot A_{in}) + S_{in} \cdot (C_{in} + A_{in}), \tag{2}$$

and the sum is derived from the inverted carry:

$$S_{out} = (S_{in} \cdot C_{in} \cdot A_{in}) + \overline{C_{out}} \cdot (S_{in} + C_{in} + A_{in}). \tag{3}$$

As indicated in fig. 3, two subsequent clocked gates reside at each signal path within either the N or the P clocked circuit area, resulting in non-inverting behavior of these areas. Hence $\overline{C_{out}}$ is derived from C_{out} between the clocked parts, and the final calculation of the sum signal S_{out} is performed by a P clocked *ANDNOR* gate. As half cycle pipeline delay



(a) N type full-adder (b) P type full-adder

Figure 2: 36 transistor low power full-adder

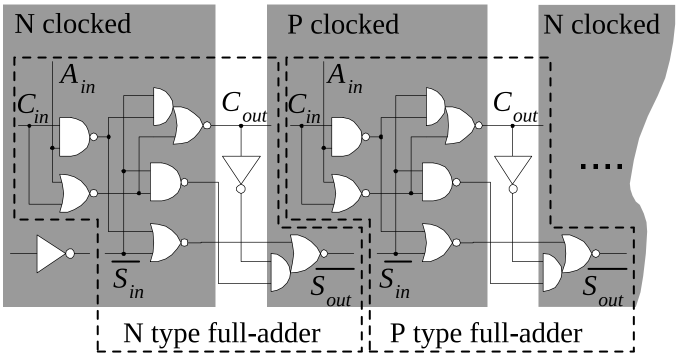


Figure 3: Pipeline scheme of cascaded full-adders

is intended, the signal S_{in} of each full-adder is expected to be delayed by a single clocked gate. The P type full-adder simply uses P clocked gates instead of N clocked ones, with the exception of the gate calculating the sum, which is N instead of P clocked. The slight increase of pipelining effort introduced by the delayed signal S_{out} is negligible for several subsequent pipeline stages, on the other hand only 6 clock transistors are required for each full-adder.

4 Comparison with Other Full-Adders

The TSPC full-adder design presented here is compared to three prior published TSPC full-adders. For each full-adder a netlist based on 0.8 μm CMOS process technology including parasitics (diffusion, routing) derived from layout has been created. The energy required for clocking is obtained by considering the full-adder clock load, the clock routing, and the energy consumption of the clock tree. Table 1 illustrates the average energy consumption during one clock cycle at $V_{DD} = 5$ V, determined by simulation using Kang's method [3] assuming statistical input signals. The full-adder design by Lu, Samueli, Yuan, and Svensson [4] manages the ultra high speed of 700 MHz for the application of a numerically controlled oscillator. Speed was improved by massive use of precharge gates and a total

Table 1: Comparison with other full-adders, $V_{DD} = 5$ V.

Full-Adder Design	Lu, Samueli, Yuan, Svensson	Somasekhar, Visvanathan	Park	This Work
f_{MAX}	444 MHz	444 MHz	227 MHz	290 MHz
Latency	2 cycle	1 cycle	1/2 cycle	1/2 cycle
Transistors	59	46	28	36
Clock Trans.	23	12	12	6
Energy/Cycle	8.95 pJ	5.44 pJ	4.54 pJ	2.35 pJ

latency of two cycles (except for the signal S_{in} which is supposed to be late by one cycle). However, speed degrades to 444 MHz when minimum size transistors are used. The one cycle full-adder of Somasekhar and Visvanathan [5] consists of 46 transistors (including 12 clock transistors), as the multiplicand register and partial product generation is omitted in the analysis given here. Considering minimum size transistors, this full-adder is even as fast as [4], but consumes less energy. A half cycle full-adder consisting of only 28 transistor was presented by Park [6], which calculates the sum by using a 3 way XOR gate. It requires 12 clock transistors and may be used as a TSPC circuit in combination with its P type equivalent. Due to the exclusive use of precharge gates the energy consumption is not significantly reduced compared to the design of Somasekhar and Visvanathan [5] . The half cycle full-adder presented here consumes almost only half the energy compared to the design of Park.

5 Conclusions

A full-adder consuming significantly less power than prior published designs is reported. This goal is achieved by constructing a half cycle full-adder, which consists of minimum size transistors and avoids precharge gates, so the resulting clock load is significantly decreased. Nevertheless, the maximum frequency is sufficient for a large field of applications.

References

[1] A. Chandrakasan, S. Sheng, and R. W. Broderson, “Low-power CMOS digital design,” *IEEE J. Solid-State Circuits*, vol. 27, pp. 473–483, Apr. 1992.

[2] J. Yuan and C. Svensson, “High-speed CMOS circuit technique,” *IEEE J. Solid-State Circuits*, vol. 24, pp. 62–70, Feb. 1989.

[3] S. M. Kang, “Accurate simulation of power dissipation in VLSI circuits,” *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 889–891, Oct. 1986.

[4] F. Lu, H. Samueli, J. Yuan, and C. Svensson, “A 700-MHz 24-b pipelined accumulator in $1.2-\mu m$ CMOS for application as a numerically controlled oscillator,” *IEEE J. Solid-State Circuits*, vol. 28, pp. 878–886, Aug. 1993.

[5] D. Somasekhar and V. Visvanathan, “A 230-MHz half-bit level pipelined multiplier using true single-phase clocking,” *IEEE Trans. on VLSI Syst.*, vol. 1, pp. 415–422, Dec. 1993.

[6] A. H. C. Park, “CMOS LSI design of a high-troughput digital filter,” master’s project, Mass. Inst. of Technol., Cambridge, ch. 4, 1984.