

10 Gbit/s Throughput Telecommunication Circuits in CMOS

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Abstract We present an architecture suitable for implementing the processing parts of high throughput telecommunication terminal equipment, in standard CMOS. A first testchip has been designed in 0.8 μm CMOS and successfully tested. It contains some critical processing parts of an SDH-regenerator. The chip process a throughput of 10 Gbit/s and is fully clocked at 622 MHz.

1 INTRODUCTION

The increasing need for higher data-rates in the fiber backbone network leads not only to interest for circuits running at the highest data-rates, e.g. multiplexers and demultiplexers. Also circuits capable of processing the entire dataflow at a lower clock-frequency is needed.

Synchronous Digital Hierarchy (SDH) is an ITU standard for transport networks. All information is packed into a Synchronous Transport Module (STM). In a 10 Gbit/s system, the SDH frame consists of 64 STM-1 frames. In a point-to-point connection, the signal has to be regenerated after a certain distance (Fig. 1). This is done by electronics, and not by optics, in order to be able to monitor bit-error-rate and other maintenance functions. The regenerator consists of a number of high-speed processing functions: e.g byte and frame alignment, bit interleaved parity (BIP) calculations, scrambling of data and add and drop of regenerator-section-overhead (RSOH) bytes. Also low speed logic for operation and maintenance is needed.

A complete STM-64 regenerator, including high speed chips, is planned. High-speed multiplexers and demultiplexers have earlier been reported [1]. Earlier reported chips for STM-64 processing has been implemented in Si-bipolar gate-array technology [2]. However, we try to integrate all processing functions in standard CMOS in order to cut cost. To be able to process 10 Gbit/s we combine both high clock frequency and parallelism. We selected to use the highest possible frequency, in this case 622 MHz. Then, a special architecture must be used in the chip design. This paper describes this architecture and the design of a first chip. Measurements on this chip are also presented.

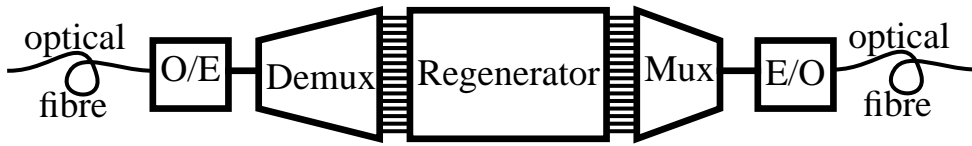


Figure 1: An example of a communication system, in which the presented architecture could be used. The regenerator is implemented in CMOS.

2 ARCHITECTURE

The architecture is mainly aimed for chips that process data with a throughput of 10 Gbit/s, but can easily be reshaped for other data-rates and applications.

STM signals are byte-oriented. Thus the signal processing must operate at some fraction of the serial byte-rate. For future scalability into higher data rates we select a clock frequency as high as possible. With a lower internal frequency the number of cells will increase, and thereby occupy a larger area. With the selected frequency of 622 MHz, we must process two bytes of data in every clock-cycle. In order to reach this high clock frequency we must employ both advanced circuit technique and good layout. Speed in CMOS logic is mainly limited by the capacitive load on each gate-output. Hence, we must provide an architecture that limits output-loads, by only allowing a small fan-out and short wires between cells.

A. The architecture

The main part of the architecture is an unidirectional datapath, consisting of cell-columns, in which the data is processed (Fig. 2). Each processing function is partitioned into an appropriate number of cell-columns, forming a processing block. All processing blocks have their data inputs on the left side, and the data output on the right side. Therefore each block transports its data rightward throughout the datapath. The height of the datapath, i.e. the number of cells in each column, is fixed to the number of parallel data-lines, in our case 16. If several functions are performed in parallel, their corresponding cell-columns must be placed interleaved in the datapath, in order to avoid long horizontal wires (function A and B in Fig. 2). A small routing channel is placed between every second column.

The main reason for this partitioning is to avoid routing long wires between cells, and thereby maximize circuit speed. The partitioning keeps connections within one routing channel, and will allow two horizontal cell-crossings at the most (Fig. 2).

With this set of rules, the maximum length of an interconnect is:

$$Length_{max} = 16 \cdot Cellheight + 2 \cdot Cellwidth \quad (1)$$

Hence, it is vital to have as low cell-height as possible. The height should be fixed, in order to provide regularity. The regular cell-size makes it simpler to use auto-routers.

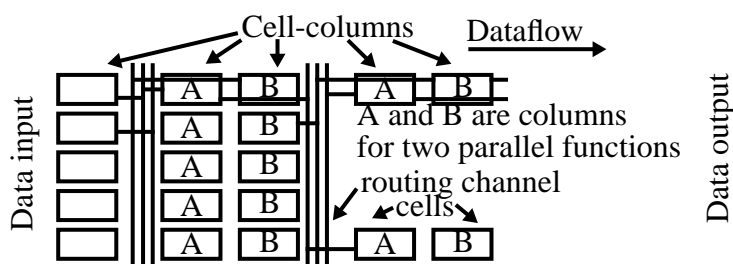


Figure 2: Schematic view of the datapath.

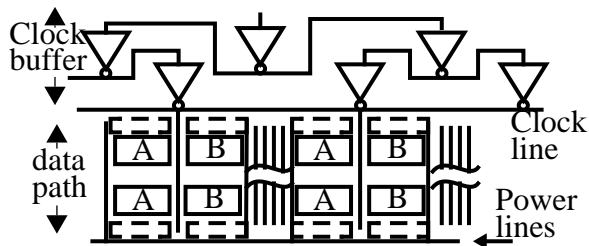


Figure 3: Clock buffer tree. Dashed boxes indicates decoupling capacitors.

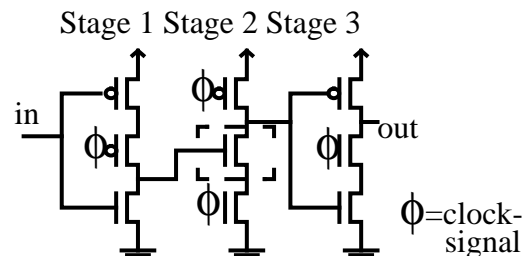


Figure 4: PET-TSPC flip-flop. Dashed line indicates the logic function.

Distribution of the clock-signal is crucial in high speed circuits. In order to obtain a high degree of timing safety, the clock-signal must arrive as simultaneous as possible to all cells. By distributing the clock-signal globally in a metal wire, with local cross-connections, the skew is kept at minimum. The clock-driver is fed by a tree of buffers, placed above and distributed along the datapath in order to achieve a radial clock-distribution for further skew reduction (Fig. 3)[3].

High clock-frequency will increase the power density, so it is important to provide a low-impedance power distribution network. The power is distributed from beneath the datapath. Thereby can clock and power distribution share a low-resistance metal layer (Fig. 3). Also here local cross connections are used to further decrease the impedance.

Noise on power lines, introduced by clock-buffers and the synchronous logic, must be reduced for high robustness. This noise is reduced by on-chip decoupling capacitors. They are placed in free cell-positions inside the datapath, and around the datapath (Fig. 3).

B. Logic style

In order to achieve a high clock frequency we must use a maximally fast circuit technique. True single phase clocked (TSPC) logic have been used in many high-speed CMOS circuits during the last few years. In order to maximize the clock-frequency we selected the TSPC Positive Edge Triggered (PET) flip-flops with integrated logic as circuit style [4]. Normally, the logic function are implemented in the precharged stage (Fig. 4 Stage 2) in each flip-flop, using three logic transistors in series at maximum. In a few cases simple logic was implemented also in the first stage of the flip-flop. Logical depths are thus ≤ 2 . One drawback of PET-TSPC is the large number of clocked or pre-charged transistors. This will lead to a relative high switching activity on many transistors, and thereby a high power consumption [5].

In a faster process it is better to select nonprecharged TSPC and a larger logical depth [4]. The power consumption will then decrease, since the number of clocked transistors, per gate function, is reduced. A faster process would also make it possible to increase the throughput by extending the width of the datapath.

3 TESTCHIP

The chip contains some critical parts of an STM-64 regenerator. It converts the STM-64 signal into 16 STM-4-like signals. Byte and frame alignment and byte to bit-stream resorter functions are included. The circuit is implemented in a standard single-poly double-metal 0.8 μm CMOS process. Chip-data are presented in Table 1. All logical blocks are verified by SPICE simulations, at worst-case parameters and a temperature of 45°C.

The chip is build from a small cell-library containing PET flip-flops with different logical

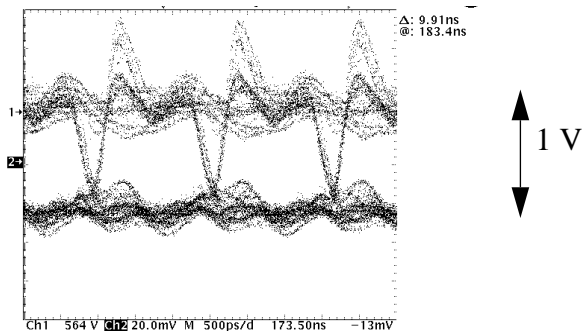


Figure 5: Output eye-diagram at 622 Mbit/s.

functions. The driving part of these flip-flops (Fig. 4 Stage 3) is separated from the logical part (Stage 1&2). Thereby it is possible to size all drivers individually after placement and routing. All cells is designed with a fixed height of 26.5 μm . The cell-width vary between 30-80 μm depending on complexity.

The clock-driver is one of the most critical part of the design. In order to fulfill the speed requirement the tapering factor in the clock-buffer must be as low as two. Also high-speed I/O is a major problem in CMOS. We used a buffer-chain at each input and open-drain outputs.

The first testchip has been successfully tested. In a CLCC-68 package we reached a clock-frequency of 622 MHz. In a high-speed package, that provides 50 Ω wires all the way to the bonding wire, it was possible to increase the frequency to 870 MHz. The circuit also accepted a supply-voltage down to 3.8 V at 622 MHz. Fig. 5 shows an eye-diagram of an output-pin on the high-speed package, measured at 622 Mbit/s. The high overshoot depends on fast turn-off in the open drain output in combination with the bond-wire inductance.

4 CONCLUSIONS

An architecture for high throughput CMOS circuits is presented. It is most useful in termination circuits in fibre-optical networks, since it is heavily pipelined. High throughput is achieved by a combination of high-speed logic and parallelism. Restrictions in partitioning, placement and cell-sizing leads to short interconnections between cells. This and fast circuit technique leads to the possibility to use a very high internal clock frequency.

From the first testchip we conclude that it is possible to implement 10 Gbit/s termination circuits in a 0.8 μm CMOS process. In a faster process, e.g. 0.6 μm , the datapath can be made several times higher. Hence, processing of data-rates of 40 Gbit/s and more can be handled in such a standard CMOS process. Also, a faster process will lead to much lower power dissipation, since the design would be more relaxed.

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Table 1 Chip characteristics

Die size	4 x 4 mm
Core size	4 mm ²
Power dissipation	1.75 W @ 5 V
No transistors	10 k
No gates	1 k
Clock frequency	622 MHz