

# An Integrated High Performance Mixed Signal IF-to-Digital Converter

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## ABSTRACT

*A single 'chip' IF-to-Digital converter containing Low Noise Amplifiers, AGC, down-conversion mixers, oscillators, baseband amplifiers, references and an A/D converter is presented. Mixed analog-digital circuit design and packaging techniques achieve a high level of integration using standard semiconductor processes. Measured results show that the IC can operate on IF signals between 30MHz-85MHz and decode transmissions up to 64QAM either in NTSC or PAL systems. Key performance factors include 63dB stable gain, 50dB IMD3, 40dB AGC range, 9dB input Noise Figure and 40Msps A/D conversion rate.*

## 1. Introduction

This paper describes a highly integrated implementation of an IF-to-Digital converter for bridging the gap between standard TV tuners and DSP chips used in the digital cable receivers or modems for decoding audio, video or data. The coaxial cable is seen in many areas as the medium for the digital TV and also the easiest ramp to the information superhighway for the PC/Internet communications. In order to utilize the standard transmission equipment the digitally encoded signals are also sent on normal 'analog' channel frequency bands. This allows the use of regular TV tuners for converting the transmissions to standard IF frequencies for NTSC or PAL. For optimum bandwidth utilization the data is transmitted in QAM (Quadrature Amplitude Modulation) format. A typical receiver or modem for decoding these transmissions as would have a standard tuner, I/Q analog down-converter, dual A/D converters and the subsequent digital processing. The tuner output is centered around a standard IF frequency and is then down-converted and digitized to recover the transmitted data and timing.

However, recent in DSP technology has enabled an all digital QAM demodulation, rendering a simplified receiver architecture as shown below in Fig.1.

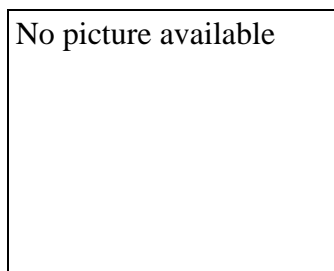


Fig.1 Pro-Digital Cable Receiver

Although the system design is simpler the requirements on the A/D converter and the IF processing circuits is more stringent leading to substantial costs and board size.

## 2. General Description

A single chip that efficiently integrates IF-to-Digital conversion is shown below in Fig.2. It performs IF amplification with gain control, frequency down conversion, frequency synthesis for mixer Local Oscillator (LO) & system clock generation, and baseband quantization with analog to Digital converter.

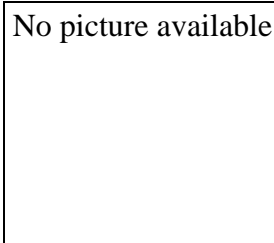


Fig.2 Functional Block Diagram of the IF-to-Digital Converter

The input directly interfaces to SAW filters and maintains low noise figure. Depending on the signal input level the gain may be controlled over a 30dB range through an external analog input signal. The gain reduction is done in two stages and orchestrated in such a manner as to minimize noise figure and signal distortion. The IF output is then down converted and filtered using a double balanced mixer. This output may be filtered even further, externally, before being quantized by the on-chip A/D converter. The digital data output can be processed to derive information for automatic gain control (AGC) and automatic frequency control (AFC). The IC is optimized to work with DSP decoders based on IF sampling. The IC also provides an optimum tuner AGC control voltage useful for controlling the front-end tuner gain.

The circuit diagram of the combined mixer-amplifier is shown in Fig.3 below. This is the core part of the front-end that down-converts the IF to baseband for A/D conversion. The output is capable of 6Vpp swing with a 12V analog supply. Measured distortion results show 50dB of IMD3. Analog sections work on 12V & 5V supplies and the digital sections work on a regulated 5V supply. The IC takes 500mW of power and is packaged in a 44-pin PLCC package.

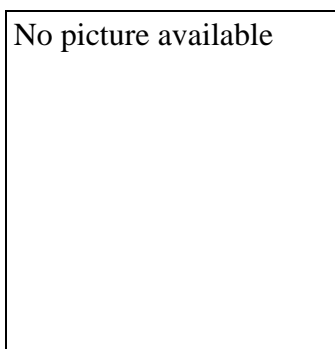


Fig.3 Mixer-Amplifier Schematic

## 3. Fabrication

Isolation between IF processing sections the ADC is achieved is by having them physically in two dies and packaging on a common substrate. This allows the high frequency analog sections to be fabricated on a mature 2u bipolar process and the A/D

on a sub-micron CMOS process. Thus the costs are greatly reduced when compared to a complex BiCMOS realization.

#### **4. Performance**

The IC has actually been tested in 64QAM receiver applications for Cable modems in both NTSC and PAL transmissions. Both IF sampling and sub-sampling architectures can utilize this integrated circuit. The BER has been acceptable while the system size and costs have been greatly reduced. Authors gratefully acknowledge C.Vinn, J.Chu, S.Lee, S.Hao and C. Reames.

#### **5. References**

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