

A power-supply decoupling method for mixed-mode low voltage, low power integrated circuits.

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This paper presents a decoupling method to achieve a good on chip power to ground decoupling with a low Q-factor. Unlike previously published methods, no resistor is added in the power supply path to reduce ringing so this method features no power voltage drop or power consumption, which makes it well suited for low voltage, low power applications.

Introduction

In high speed mixed-mode IC's, an adequate decoupling is primordial to achieve the projected specifications. Due to the bondwires' inductance, fast current changes cause on chip variations of the power supply voltage relative to the on chip ground reference. This causes stringent Power Supply Rejection Ratio (PSRR) specifications for the integrated analog circuits. An even tougher problem is the injection of substrate noise through power supply to substrate capacitances which may disturb any analog circuit integrated on the same chip. The *on chip* power-supply to ground voltage has therefore to be kept as constant as possible.

Power supply decoupling can be analyzed in the frequency domain. Any circuit which consumes a non-constant current generates a voltage on the power to ground impedance. Due to the inductance of the bondwires, the impedance between on chip power and ground is large at high frequencies. To reduce this impedance, an internal decoupling capacitance (C_{decop1}) can be used. This is added to the circuit capacitance (C_{cir}) between power and ground which is formed by the overlap between power and ground tracks, the well-substrate junction capacitance and the transistor capacitances. At frequencies where the bondwire impedance is becoming noticeable, any large off-chip decoupling capacitance can be considered as a shortcut. The impedance between on chip power and ground is a parallel circuit of the on chip capacitance ($C_{\text{decop1}} + C_{\text{cir}}$) and the bondwire inductance (Figure 1). This is a resonant circuit featuring serious peaking which can also be observed in the transient response of the power to ground voltage. The high Q-factor causes ringing which takes a long time to extinct. To reduce the Q-factor a resistor can be added in series with the bondwire^[1]. This reduces the ringing, but results in a DC-voltage drop in the power line and power loss, which makes this method unsuitable for low voltage, low power applications. This paper presents an alternative method to achieve a small power to ground impedance with little ringing and without the voltage drop penalty.

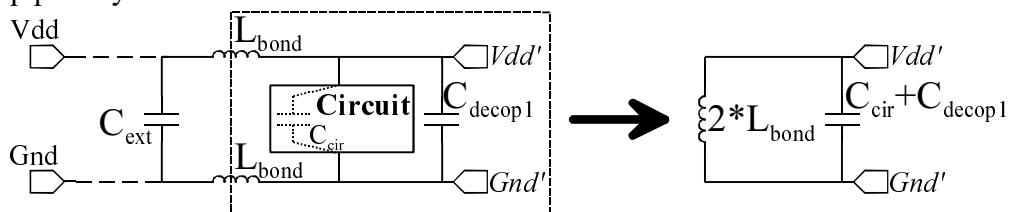


Figure 1 : The LC resonant circuit in traditional on-chip decoupling

The RLC decoupling method

The frequency response of the power to ground impedance on chip (Vdd' to Gnd' in Figure 1) with C_{decop1} included in C_{cir} is presented in figure 2. The resonant peaking occurs at

$$\omega_{peak} = \frac{1}{\sqrt{2 \cdot L_{bond} \cdot C_{cir}}} \quad (1)$$

Instead of adding a resistor in the power path to eliminate the peak, a circuit with opposite resonance is added in parallel to the original parallel LC-resonant circuit. This is formed by a serial connection of L_{decop} and C_{decop} (Figure 2). Both circuits have the same resonant frequency if

$$2 \cdot L_{bond} \cdot C_{cir} = 2 \cdot L_{decop} \cdot C_{decop} \quad (2)$$

In this equation the decoupling inductor $2 \cdot L_{decop}$ is split in two parts. This is not necessary, but it can be useful if bondwire inductors are used as will be explained later. If one assumes that

$$C_{cir} = X \cdot C_{decop} \quad (3)$$

the power to ground impedance of the decoupling circuit is given by:

$$Z = \frac{2j \cdot \omega \cdot \frac{L_{decop}}{X} \cdot (1 - 2 \cdot \omega^2 \cdot L_{decop} \cdot C_{decop})}{(1 - 2 \cdot \omega^2 \cdot L_{decop} \cdot C_{decop})^2 - 2 \cdot \omega^2 \cdot \frac{L_{decop} \cdot C_{decop}}{X}} \quad (4)$$

This features however two extra resonant peaks (Figure 2). As this peaking is obviously as unwanted as the peaking with a single decoupling capacitance, some resistance R_{decop} is added in series with L_{decop} and C_{decop} . This resistor is not in the power-path so no voltage drop or DC power loss is introduced. The global circuit diagram is presented in figure 3. The optimal value of R_{decop} is obtained when both peaks converge to a flat top (Figure 2). When equation (2) is fulfilled the resonant peaks spread as L_{decop} gets smaller and C_{decop} larger. This doesn't mean however that the inductor should be omitted, as a zero inductance corresponds to an infinite capacitance which is obviously unfeasible.

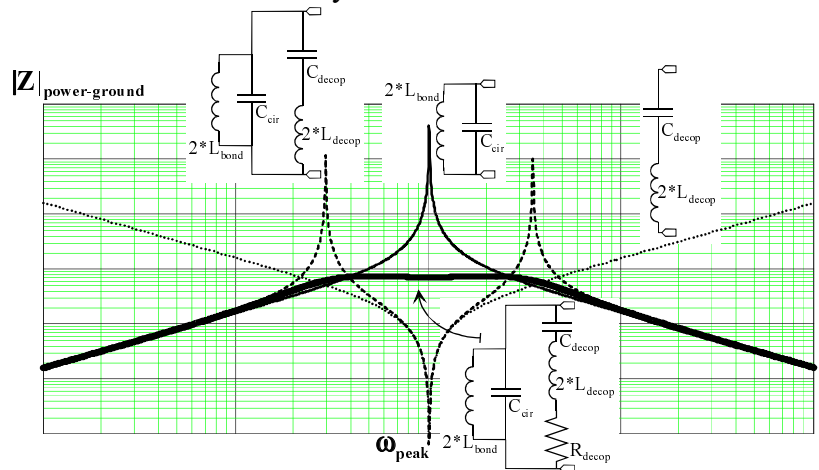


Figure 2 : Frequency response of the various on chip power to ground impedances

The major advantage of the presented scheme over traditional on chip decoupling capacitance is the greatly reduced quality factor of the resonant power to ground impedance without adding a resistor in the power path. As an example for a circuit which consumes 100 mA, a resistor of only 10Ω in the power path results in a voltage drop of 1 V and a power loss of 100 mW. This is 20 % power loss with a 5 V power supply. The presented technique is therefore very well suited for low voltage, low power applications. Figure 4 compares the

presented method with a single on chip capacitance and a capacitance with a $10\ \Omega$ resistor in the power path.

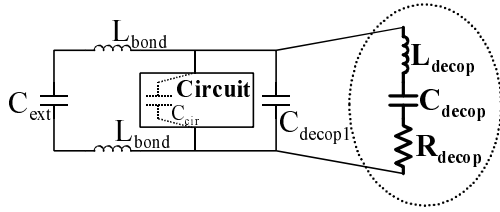


Figure 3 : Circuit diagram of the presented decoupling method

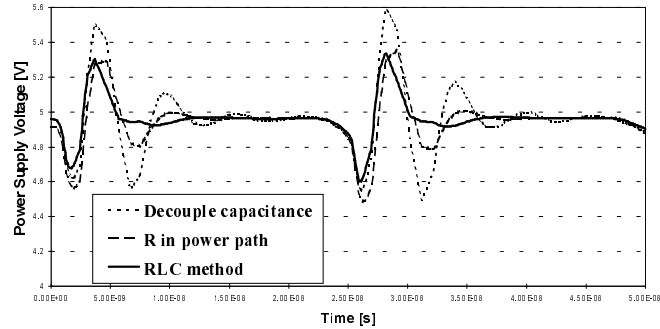


Figure 4 : Simulated power supply with various decoupling methods

Realization of the presented decoupling method

The presented scheme can be implemented in several ways. The most adequate depends on the required results and the available surface on chip. In traditional on chip decoupling circuits, extra capacitance is added in spare places between power and ground lines. This will mainly shift the resonant peak to lower frequencies without reducing the Q-factor a lot. As this capacitance is placed parallel to C_{cir} , it is considered as a part of it. It is useful in the presented scheme, since a larger C_{cir} corresponds to a higher optimal $C_{decop} * L_{decop}$. The optimal R_{decop} for this combination is smaller resulting in an overall smaller impedance.

If sufficient space is available to integrate a capacitor C_{decop} much larger than C_{cir} , a decoupling capacitance with only a series resistance R_{decop} will already significantly reduce peaking. Adding a small inductor will reduce the Q-factor even further which results in shorter ringing. This is especially useful in sample and hold based systems, where the sampling can occur when the ringing has disappeared. If C_{decop} on chip can not be larger than C_{cir} , a single resistance in series with C_{decop} is insufficient to reduce the Q-factor significantly. The presented RLC decoupling scheme is then indicated to reduce the Q-factor without power supply voltage or power loss.

Inductor L_{decop} can be realized as an on-chip spiral inductor^[2]. As a resistor is added, a very small internal resistance is not required and the spiral inductor can be kept relatively compact. A 20 nH spiral inductor will take about $(100\ \mu\text{m})^2$. This surface corresponds to a capacitance of about 20 pF. As stated before a larger capacitor and a smaller inductor, fulfilling equation (2) feature the best results. When the surface is limited however, it can be necessary to replace some capacitance for inductance as the capacitance is proportional to its surface and the inductance to its surface^{3/2} [3].

As L_{decop} is of the same order of magnitude as L_{bond} , a bondwire can be used as inductor^[4]. In the special case where the decoupling capacitance is comparable to the intrinsic circuit capacitance, a bondwire from the die to the chip package and back to the die (Figure 5) will have a good inductance value. It is also possible to use an off-chip decoupling capacitance, with the connecting bondwires as inductors. Very good results can be obtained with an SMD decoupling capacitance placed *in* the chip package (Figure 6). Thanks to the proximity of the capacitance to the die, L_{decop} is small compared to L_{bond} , so the capacitance can be large, which gives a flat frequency response over a large frequency range. The capacitance can eventually be placed external to the package and is then about as large as C_{cir} . It must not be misinterpreted as an extra off-chip decoupling capacitance which could be placed in parallel with the original off-chip decoupling capacitance. It is merely used for a flattening of the *on-chip* impedance between power and ground.

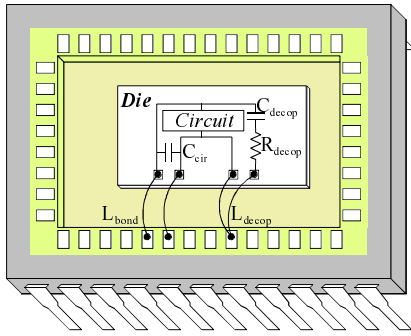


Figure 5 : Bondwire used as L_{decop}

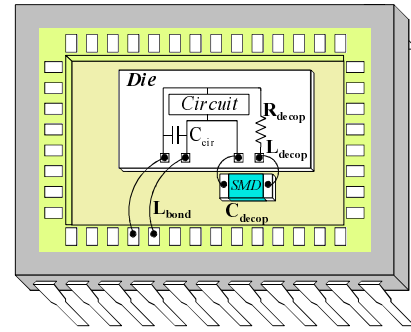


Figure 6 : SMD capacitor used as C_{decop}

In the ideal case, equation (2) should exactly be fulfilled. To consider spreading on C_{cir} and L_{bond} , some safety margins should be taken into account. C_{decop} is best designed somewhat too large without considerable decoupling degradation.

Testchip and measurement results

A testchip has been realized to test the presented decoupling method. It consists of several large inverter strings which represent some digital circuitry. The inverter string is triggered externally. Various decoupling schemes were implemented on the chip. To measure the relative variation of power to ground on chip, a differential amplifier is implemented (Figure 7). The variation of the power supply voltage relative to the on chip ground is passed through C_{pass} to M_1 . This voltage is converted into a current which flows through R_{meas} , the 50Ω input of a scope. The scope display is the relative variation of power to ground on chip. In figure 8 the measured power to ground voltage of a traditional decoupling capacitance and the presented scheme are compared. In the testchip bondwire inductors are used. The presented decoupling schemes yields the lowest peak-to-peak voltage and shortest ringing as expected and this without resistors in the DC power path.

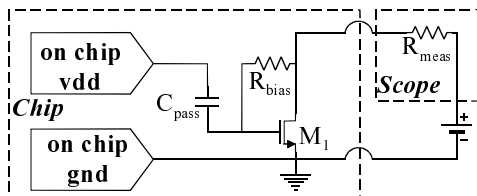


Figure 7 : Differential amplifier to measure power to ground voltage variation

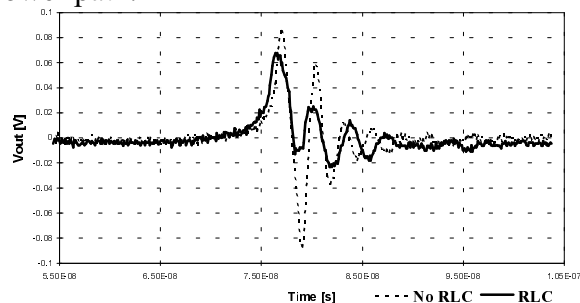


Figure 8 : Measured on chip power to ground noise due to switching of an inverter string

Conclusion

A decoupling procedure has been introduced which features a low Q factor of the power to ground impedance without adding resistive elements in the power supply path, unlike previously published solutions. The lack of DC voltage drop and power loss makes this method especially suitable for low voltage, low power mixed-mode applications.

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