

A Low Voltage Evaluation of a 1.9 GHz Silicon MOSFET Gilbert Cell Downconversion Mixer

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Abstract - The mixer presented has the highest reported frequency of operation for a CMOS mixer (1.9 GHz) and the lowest reported noise figure for a CMOS Gilbert cell mixer (SSB NF of 7.8 dB). The paper describes a 1.9 GHz monolithic double balanced Gilbert cell downconverting mixer, fabricated with a standard 0.8 μm CMOS process, operating over a range of supply voltages from 1.8 V to 5 V. The mixer has conversion gain at 1.9 GHz for voltages as low as 1.8 V with a LO drive of -8 dBm while dissipating 4.3 mW in the Gilbert Cell.

1. INTRODUCTION

A CMOS RF stage would allow a considerable increase in transceiver integration and a reduction in transceiver cost. Recent CMOS mixers have employed a singly balanced cascoded N and P channel Gilbert cell topology which takes advantage of excellent current reuse, however, the use of P-channel devices limits the frequency of operation [1]. Resistive and commutating MOSFET mixers have excellent IP3 but poor conversion gain, poor noise figure and also demand high LO drives of greater than +10 dBm [2]. The Gilbert cell employs an all N-channel topology and requires modest LO drive requirements to achieve reasonable conversion gain and noise performance. This paper investigates the

low voltage capability of a MOSFET Gilbert Cell downconverting mixer to demonstrate CMOS as a potential RF technology.

2. GILBERT CELL MIXER DESIGN

A reduced LO drive is a significant advantage in low power IC design because; large LO signals result in an increase in power dissipation and a reduction in LO-RF/ LO-IF isolation. A doubly balanced Gilbert cell mixer was designed requiring reduced LO power, Figure 1, with no source degeneration in the tail of the differential amplifier section. The mixer configuration was optimized for conversion gain and noise figure rather than linearity or intercept point IP_3 . The current of the downconverting mixer is controlled by current mirrors that regulated half of the total current to the Gilbert cell mixer and half the current to a differential source follower IF buffer. The source follower output stage was required to match the mixer output impedance to the 50Ω measuring device. The downconverting mixer was fabricated in a standard $0.8\ \mu\text{m}$ minimum gate length (drawn) CMOS process and the entire mixer had an active area of less than $0.15 \times 0.15\ \text{mm}^2$. The gate-source threshold voltage for the n-MOSFET's was $0.7\ \text{V}$ and no special channel implants were used to lower the threshold voltage. A salicide process and the physical layout of multiple gate fingers aided in the reduction of gate resistance which improved the MOSFETs high frequency performance [3].

3. MEASUREMENTS

The mixer was tested in a 24-pin, plastic surface mount, SSO-24 package. All measurements were performed with differential LO and RF signals; a total of 10 pins were required to evaluate the mixer. The SSO-24 package was surface mounted on a standard fiber glass printed circuit board (FR4-PCB). On the PCB, 50Ω microstrip lines were mated to the narrow pitch pins of the SSO-24 package and to SMA connectors that enabled measurement. The RF and LO ports were matched to 50Ω on the PCB board. The bias points for the RF and LO ports were provided off chip through $10\ \text{K}\Omega$ resistors. The IF signal of the down converter was fed off chip differentially into the primary of a 2.2:1 balun, which transformed a differential IF output impedance to a single ended 50Ω impedance for measurement.

A plot of conversion gain and single-side band noise figure (SSB NF) over different current levels is displayed in Figure 2 for a supply voltage of $2.7\ \text{V}$. The measured peak conversion gain was $5.5\ \text{dB}$, the minimum measured SSB NF was $8.8\ \text{dB}$ @ $\text{RF}=1.9\ \text{GHz}$, $\text{LO}=1.65\ \text{GHz}$. The general trend of maximum gain occurring during minimum noise figure

held for all supply voltages measured. The noise figure had a broad minimum as a function of current while the conversion gain was more highly dependent on the current. An input third order intercept point of -3 dBm is displayed in Figure 3 for a voltage supply of 3 V. Conversion gain and SSB NF versus LO power is displayed in Figure 4: For a voltage supply of 2.7 V, the maximum conversion gain was 5.5 dB and the minimum SSB NF was 8.8 dB with an associated LO drive of -8 dBm.

Measurements were taken over a variety of power supply voltages (V_{dd}). For a set power supply voltage, conversion gain and SSB NF was optimized by adjusting the LO input power, current and the DC bias points of the LO and RF input points. Once optimum NF and conversion gain were attained, two tone IP_3 measurements, single tone -1 dB compression, conversion gain and single-side band noise figure measurements were taken. The complete results for the optimum noise figure and conversion gain over supply voltage are displayed in table I. Some highlights from table I include; with a 5 volt supply the mixer had a conversion gain of 9.7 dB, a SSB NF of 7.8 dB and an iIP_3 of -1.0 dBm. With a 1.8 volt supply the mixer had a conversion gain of 0.5 dB, with a LO drive of -8 dBm, a SSB NF of 10.2 and a iIP_3 of -6 dBm, while dissipating 4.3 mW in the Gilbert cell and 4.3 mW in an output buffer. As the supply voltage and power is increased noise figure and iIP_3 improve resulting in higher dynamic range for the mixer. The CMOS mixers input -1 dB compression point seemed to follow a -9 dB rule with respect to the iIP_3 point.

4. CONCLUSION

The 1.9 GHz MOSFET Gilbert Cell mixer presented has conversion gain and very good SSB noise figure while operating at supply voltages as low as 1.8V. The reduced LO power requirement and low voltage operation make the MOSFET Gilbert Cell look attractive for a low voltage all CMOS transceiver.

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[2] Crols J., Steyaert S. J. "A 1.5 GHz Highly Linear CMOS Downconversion Mixer" IEEE Journal of Solid State Circuits, Vol. 30, No. 7, July 1995.

[3] Voinigescu S. P., Tarasewicz S. W., MacElwee T. and Ilowski J., "An Assessment of State-of-the-Art 0.5 μ m Bulk CMOS Technology for RF Applications" IEDM, pp. 721-724, 1995

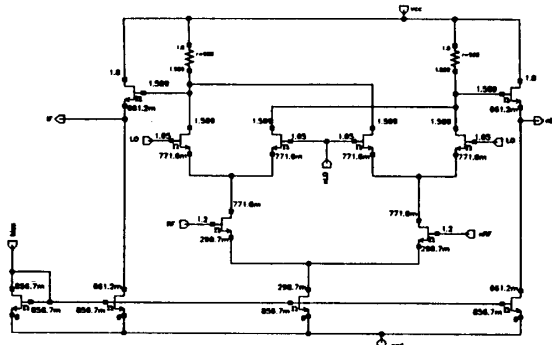


Fig 1. Schematic and DC Bias Points at 1.8 Volt Supply

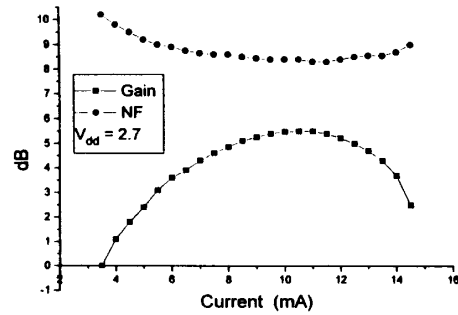


Fig 2. Noise Figure and Conversion Gain vs Current

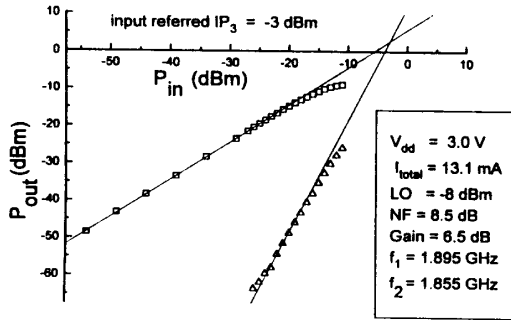


Fig 3 input IP₃ Measurement

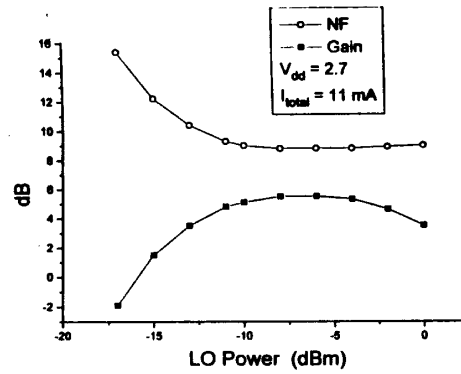


Fig 4. NF and Conversion Gain verse LO Power

Gain Conversion and Noise Figure Optimized over Supply Voltage

Supply Voltage	V	1.8	2.1	2.3	2.5	2.7	3.0	4.0	5.0
Total Power Dissipated	mW	8.6	12.2	15.9	23.0	29.7	39.3	82	133
LO Power (1.65 GHz)	dBm	-8	-8	-8	-8	-8	-8	-5	-3
SSB NF (50Ω)	dB	10.2	9.4	9.0	9.0	8.8	8.5	8.2	7.8
Conversion Gain	dB	.5	2.4	3.7	4.7	5.5	6.5	8.7	9.7
Input IP ₃	dBm	-6	-5.5	-5	-4	-3.5	-3	-1.5	-1
Input -1 dB Compression	dBm	-15	-14.5	-14	-13.5	-13	-12	-10	-9
Bias Voltage on LO Port	V	1.65	1.7	1.8	1.9	1.95	2.0	2.6	3.48
Bias Voltage on RF Port	V	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.25

RF Frequency = 1.9 GHz , IF Frequency = 250 MHz