

High Speed Content Addressable Memory

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Abstract:

A high-speed associative memory is described which is embedded in a newly developed processing unit chip. The size of the associative macro is 1.5 mm^2 . The edge size of the chip is 14.6 mm. It is one of 6 chips of a S/390 microprocessor chip set. The technology used for the chip set is $0.35 \mu\text{m}$ CMOS with 6 levels of metal.

1. Introduction

The CAM macro had to be designed for a processing unit chip in which it is used to look up absolute addresses of the L1 Cache. In case the looked up address is found, it will be marked up in the CAM. Then this information will be read out, and the access to the address of the L1 Cache will be prohibited. There are 4 of these CAMs in the PU. Each CAM has 2×128 entries with 24 bits for each entry. A special layout structure, an optimized circuit design and a modern technology resulted in a high-performance array with a typical access time of 1.1 ns. On the dense PU chip, multiple custom macros are embedded, e.g. an L1-Cache, L1-Directory, Data Local Store, Translation Look-aside Buffer and a Read Only Store. There is an additional amount of 450.000 logic gates on the chip which are automatically placed and wired. This adds up to 7.2 million FETs and 127 meters of global wiring.

2. Process Technology

The used process is a CMOS process which is called CMOS5X. The minimum structure resolution is $0.35 \mu\text{m}$ resulting in $0.25 \mu\text{m}$ effective gate length. The electrically effective thickness of the CMOS gate oxide is 7.7 nm. The two-way NAND gate delay (FO=2, 2 mm wire) is 145 ps. The process includes five levels of metal for global wiring and one additional level of metal for local interconnects. The internal circuits and macros operate at 2.5 volts, while the interface is provided by dual 2.5/3.3 volt I/O circuitry. Such high performance applications are favored by the traditional flip-chip technology and by multilayer ceramic (MLC) substrates. The CAM macro is designed as full-custom macro and prepared to be used in a CMOS5X ASIC environment. This means densities of up to 1.6 million gates per chip, 748 packaged signal pins and 340 power pins.

3. Block Diagram

The CAM macro (Fig. 1) consists of two parts: The CAM part (1 write port) can store 256 words of 24 bit length. If Clock, D-DATA, Write-D and 7 address bits are applied, 24 bits can be written into 1 of 256 entries. The SRAM part (1 write/read port) can store 1 bit into one of 256 locations. There is, however, a second access to the SRAM part via the Enable circuits. In case of an associative search (IOM and Clock are active), only the 24 bits of Compare Data are activated. They are compared with the 256 entries. In case of a match with an entry, the respective Hit/Miss Line sets the corresponding invalid bit in the SRAM field via the Enable circuit. In the next cycle, 2 of the questionable bits can be read out.

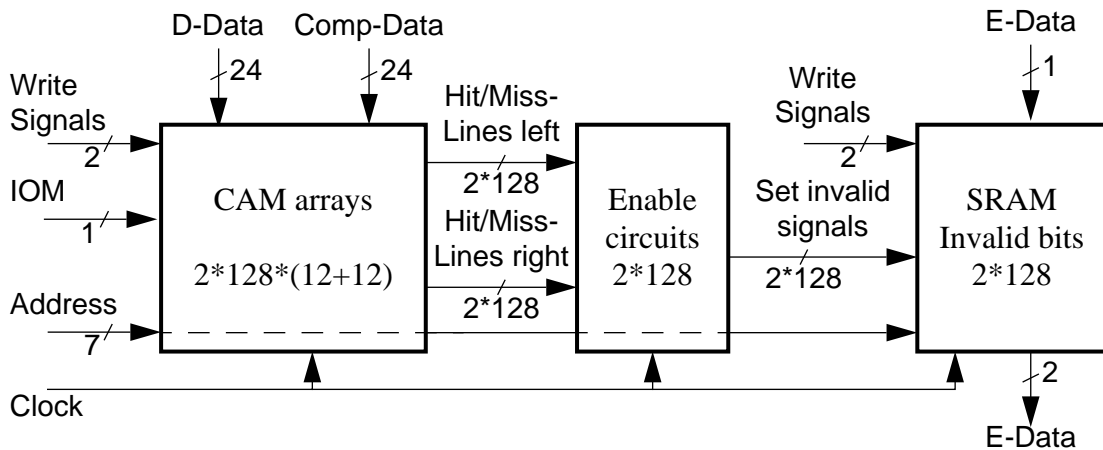


Fig. 1: The block diagram of the CAM

4. Circuit Description

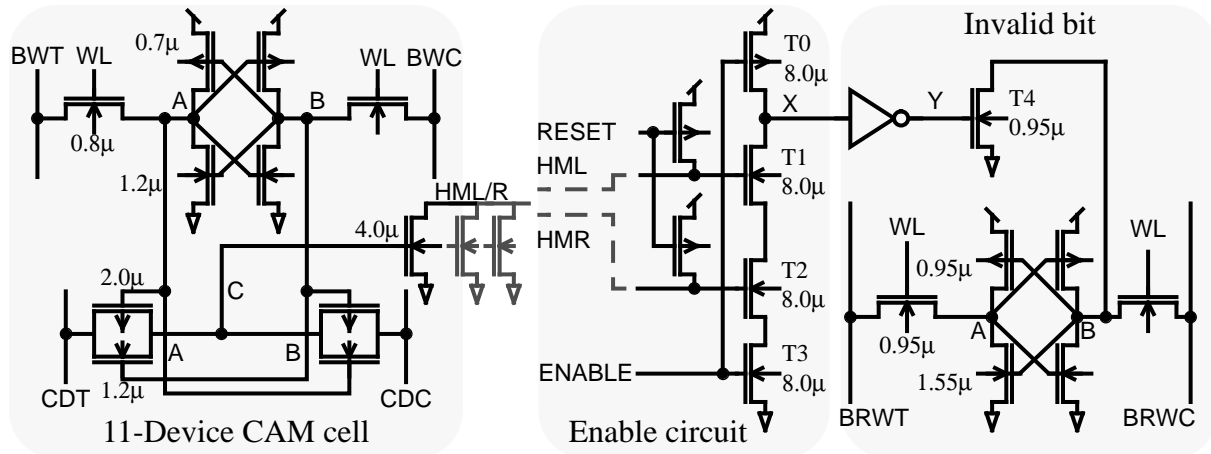


Fig. 2: CAM cell, Enable circuit and SRAM cell for the Invalid bit

- The CAM Cell

The basic CAM cell is a 6-device-cell with an attached XOR-Gate built-up out of 4 transfer devices (see Fig.2). The cell is a rather conventional one. Much attention has been given on stability of the cell due to possibly high soft error rates. With smaller cell designs, fewer alpha particles hit the cell area, but more of them cause fails.

Data is written into the cell quite traditionally via the bitlines BWT or BWC. The associative

search is performed by pulling the true (CDT) or complement (CDC) compare line high. Thus, the match transistor T1 is either in On-state (no match) or in Off-state (match). The drains of 12 match transistors are tied together to the line HML or HMR (see also Fig. 2). If one of 12 match transistors is in On-state, the precharged match line is discharged to a low potential.

- The Enable Circuit

The Enable Circuit (Fig. 2) is designed to combine the content of the 2 match lines, to restore both match lines at the end of each cycle (by RESET), to gate the signal at the appropriate time (by ENABLE) and to amplify the signal (X to Y) which is used to write the SRAM cell.

- The SRAM Cell

The SRAM cell is a conventional 6-device-cell plus one NFET which is used to pull node B down to ground potential, if a match in the appropriate entry has occurred. When the NFET T4 is active, all wordlines (WL) have to be inactive. This content of the cell can only be changed by a new write cycle, and it can be read out by a normal read cycle.

5. Layout

The layout work was driven by an IBM-proprietary layout & checking system, which guaranteed that no groundrule errors and no logical to physical differences remained after the design was completed. Fig. 4 shows the floorplan of the CAM macro. The main goal during layout, besides the goal of staying free of errors, was to optimize the performance. This means not only to design for fast access and cycle times but also to provide a safe design with low soft error rates and good noise tolerance. For speed, we chose short bitlines (64 bits long) with lowest possible capacitance, low resistivity signal lines, optimized buffers for long lines and high loads, and well tracking internal clock signals which are generated in one circuit only (timing chain).

With the advantage of having 6 wiring levels, we decided to use only 4 of them and to save the last two levels for global wiring which are allowed to run across the macro and to pick-up the macro inputs and outputs directly at the location where they end. So, it was not necessary to lead the input/output signals to the macro border for picking them up. The next chapter will deal with the item noise tolerance.

Two identical array halves were designed which were mirrored at the Y axis. Thus, with a proper organization during designing a lot of work has been saved. Special circuits like the unique timing chain and word decoders have been added afterwards.

6. Noise Immunity

The small dimensions allowed by the CMOS5X technology and the steep slopes induce noise and cross-coupling problems. Therefore the following measures have been applied to prevent the CAM macro from being noise sensitive.

- Bitline crossing: Bitlines and compare data lines are crossed three times, reducing the influence of neighboring lines essentially. The areas with the bitline crossing also contain N-well and substrate contacts as well as additional power rails.
- Circuits which are not needed during special modes are being made inactive. They are not switching and do not contribute their own noise: e.g. during the associative search, the address system, all wordlines, the bitlines, the sense amplifiers and output circuits are idling.

- Hit-/Miss-lines are always orthogonally running to global chip wiring on the upper level.
- Stable storage cells can stand high Q_{crit} (critical quantity of charge).
- The circuits on the macro have been specially checked not to allow surge currents, if NFETs and PFETs are leading currents at the same time (DC path).

Outside the macros, the following precautions are made to improve the noise immunity:

- The length of the automatically wired signal lines is controlled and, if necessary, reduced.
- Long clock lines are not wired in parallel.
- There is a high number of power pads on the chip. This allows a high number of output circuits to be simultaneously switched. But they are generating a lot of noise, and have to be observed very carefully.

7. Testing and Results

The CAM macro is tested in two ways. Firstly by the 'Array-Built-In-Self-Test' (ABIST), secondly by a random pattern test. Some additions to the design were necessary to perform the ABIST-Test, like multiplexers and observation latches at all inputs and scannable latches at the outputs using specific clocks. An additional logic macro offers basic test patterns and even senses the access time. This test is the main test which is both applied during chip production and during system start-up directly after power-on. The random pattern test is only needed for special analyses.

The CAM macro was embedded on a testsite and was found to be fully functional. Numerous measurements were taken to check the validity of the project assumptions. The width of functional margins was remarkable: The macro functions were verified between 1.6 V and 4.3 V for the supply voltage and between 10 °C and 100 °C device temperature. The nominal access time of 1.1 ns at 2.5 V varied by $\pm 17\%$ on 5 wafer lots.

8. Conclusion

A CAM macro was designed meeting the requirements of a S/390 microprocessor chip set. The macro functions were verified on hardware, confirming circuit simulation results. The embedding of the macro together with other macros and the automatically wired logic circuitry on the PU chip has been completed.

9. Acknowledgments

The authors would like to thank Dr. C.W. Starke for his encouragement and K.J. Getzlaff, H.W. Tast, O.M. Wagner, H.G. Zipperer and M. Strohmer for their assistance.

10. References

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