A 0.9V Microcontroller for Portable Applications

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A 0.9V to 1.6V, 1MHz, 8 bit microcontroller based on the 68HC08 architecture is presented. In addition to standard digital microcontroller functions, the chip features RAM, ROM, PLL clock synthesis, and LCD drive capabilities operating from the voltage supply range of a single AA or AAA battery.

1 Introduction

Portable applications, expected to dominate the future electronics markets, use batteries as energy source. The battery life time is an essential competitive factor. To optimize the consumption of electric charge, it is desirable to use integrated circuits able to operate directly from the voltage provided by the battery . This paper demonstrates an 8-bit microcontroller based upon the 68HC08 architecture [1], operated on an one-cell battery. The main features of the chip are summarized in Table 1.
All circuitry preserves functionality and meets performance specifications over the entire voltage supply range as it drops from 1.6 to 0.9V. The processing technology used for the microcontroller is a modified CMOS technology featuring unilateral devices and is described elsewhere as LV-GCMOS[2]. The main device characteristics are listed in Table 2.

Table 1: Microcontroller features	
Architecture	M68HC08
Main blocks	CPU, PWM, SCI/SPI, Clock Generation Module, LCD Drivers, SRAM, ROM
Operating voltage	0.9V - 1.6V
Bus frequency	1 MHz
LCD driver levels	0x to 3x Vsupply
Die size	6.2 x 6.2 mm2

Table 2: LV-GCMOS @1.2V	N	P
Threshold voltage (mV)	541	521
Transconductance (µS/µm)	23	6.2
Idss (pA/µm)	.31	0.08
Idsat (µA/µm)	52.3	15.6
Subthreshold slope (mV/dec)	73	77
Body effect (mV)	77	87
DIBL (mV/V)	29	19.4
Leff (µm)	0.53	0.5

2 Blocks design

The microprocessor design is based upon a block-based semi-custom approach.The pre-existing library of CMOS modules has been carefully evaluated with respect to its low voltage performance. It was determined that several logic blocks designed using either full custom or cell-based methodologies would fulfill the specification when migrated to the new process. To convert existing CMOS designs to LV-GCMOS, it is necessary to identify the source from the drain in the unilateral devices. Two semi-automatic software approaches have been implemented. The heuristic method comprises layout database inspection, starting with the assumption that any electrode connected to a power rail is a source and then working step by step, solving conflicts either by additional rules or by selecting the alternative yielding the higher speed. An alternative method inspects the

schematic checking the correctness of orientation, reversing the CMOS transistors for which the criteria are violated (Fig 1).
The embedded memory blocks available in the library did not yield the required performance when converted to LV-GCMOS. Therefore, the memories have been submitted to detailed optimization studies including structures generated by CMOS memory compilers and new manual designs. The SRAM block selected for the final microcontroller structure was a new design using a sub-block enabling technique to considerably reduce the switched capacity, combined with de-glitching latches on all outputs and a judicious architecture for multiplexing columns and sensing [3]. In total, the new low voltage design was about half the power of the direct conversion and comfortably exceeded the speed requirement at 0.9V. The SRAM showed full functionality at usable speed down to 0.7V. The ROM block selected for the final microcontroller structure was generated with a proprietary compiler as a CMOS design and then converted to LV-GCMOS. It has been specified tall and skinny to optimize the chip floorplan.
For a reasonable display contrast it was necessary to include a charge pump generating multiples of the supply voltage (2 VDD and 3 VDD). Four external capacitors have been necessary to store the charge. The charge pump was functional over a supply voltage range from 0.6V to 1.8V, achieving an efficiency better than 97%. A novel logic style was implemented to switch the charge pump from start up to operating mode thus limiting gate oxide stress in both modes to less than 3.4V (Fig. 3). The LCD drivers included level shifters between the registers storing the pixels to be displayed and the output stages. The output stages have been built using cascoded devices. Akin to the charge pump, driver switching sequences have been carefully timed, such that no transistor is exposed at any point in time to a voltage higher than twice the supply voltage to eliminate any potential reliability risks.
A particular challenge was to design the clock generator to cover the whole voltage range. A structure using a second order filter, PHD, VCO and a divider has been designed to work from 77kHz to 10 MHz. Adequate compensation techniques ensured sufficient accuracy of the current reference and careful linearization of the VCO gain curve resulted in improved noise performance over an available CMOS design specified at 1.8V.

3 Chip design

The chip photograph is shown in Fig. 4. It is visible that the relatively large capacitance of the on-chip bus represents a challange for meeting the speed specification. Parasitic evaluations indicated that the bus drivers will have to switch a load capacitance higher than 6pF. In order to avoid the bus becoming the system bottleneck, a logic block with the function of a bus splitter was added on the chip buffering blocks with single cycle requirements from blocks with less stringent timing.

4 Experimental results

The microcontroller met the specification in all respects, passing all tests under worst case process variation, temperature [4] and supply voltage. The CPU performance in this implementation is illustrated in Fig. 5, Fig. 6 and Fig 7. It is interesting to note the very low leakage current, an essential parameter for portable systems spending signifcant portions of time in a stand-by mode of operation. Furtermore, when plugged in a pager, the controler was able to decode and display messages.

Acknowledgments

The Integrated Development Fab and the Low Power Device Engineering groups in the Advance Custom Technologies Lab SPS Technology, are acknowledged for building devices and ICs, Karen Hendricks and Paul Kelly, Paging Products Division, MIMS, have been instrumental in testing the ICs, Tim O'Connell, High End Operation, MMTG, SPS compiled the CMOS memories.

References
[1] "CPU08 Reference Manual", CPURM/AD, Motorola, 1993.
[2] J.P. John et al., "A Low Voltage Graded-Channel MOSFET (LV-GCMOS) for Sub-1V Microcontroller Applications", to be presented at the "1996 Symposium on VLSI Technology".
[3] James S. Caravella, “A Low Power One Volt 4kB SRAM Design for Embedded Applications”, submitted for publication.
[4] C. Park et al., "Reversal of Temperature Dependence of Integrated Circuits Operating at Very Low Voltages", IEDM Technical Diges, p. 71, 1995.

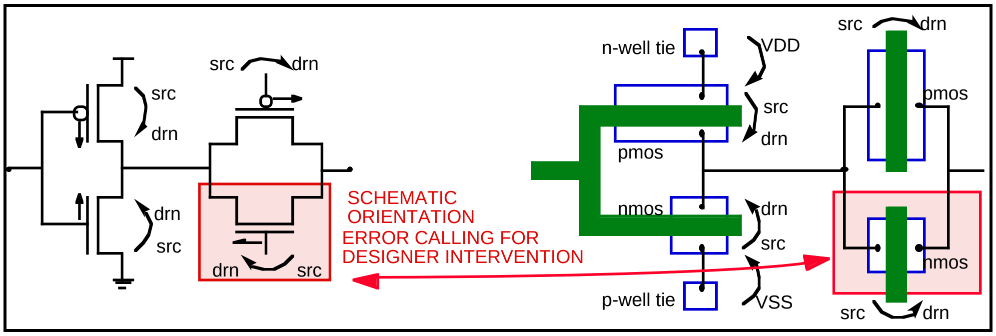


Figure 1. CMOS to LV-GCMOS Unilateral Device Mapping.

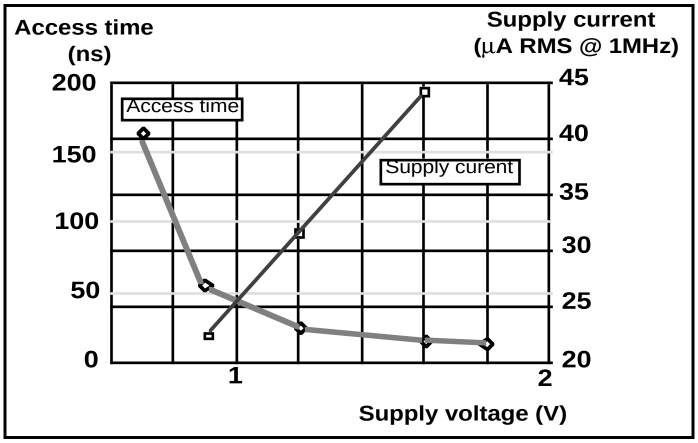


Figure 2. 512kB embedded SRAM performance measured on a stand-alone test structure.

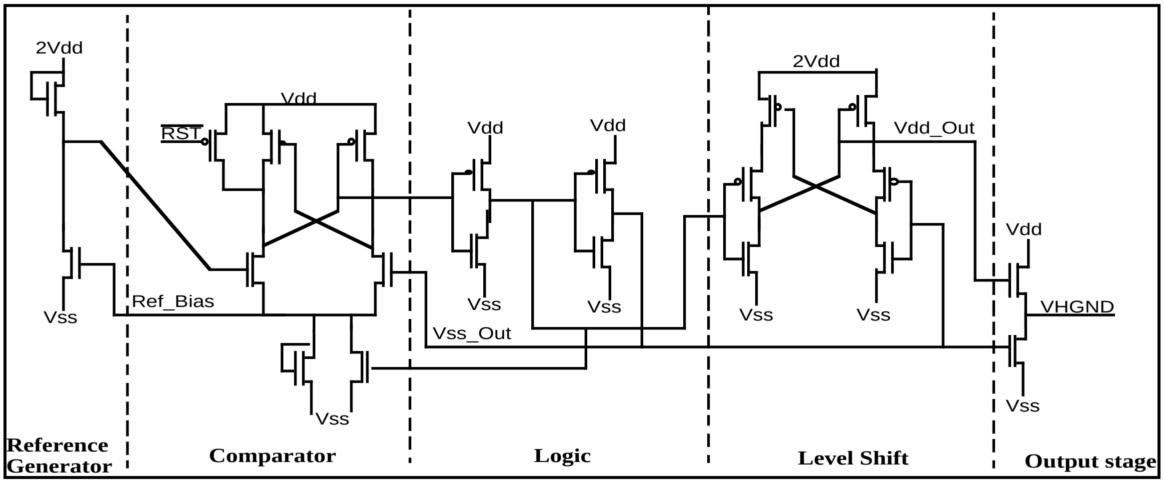
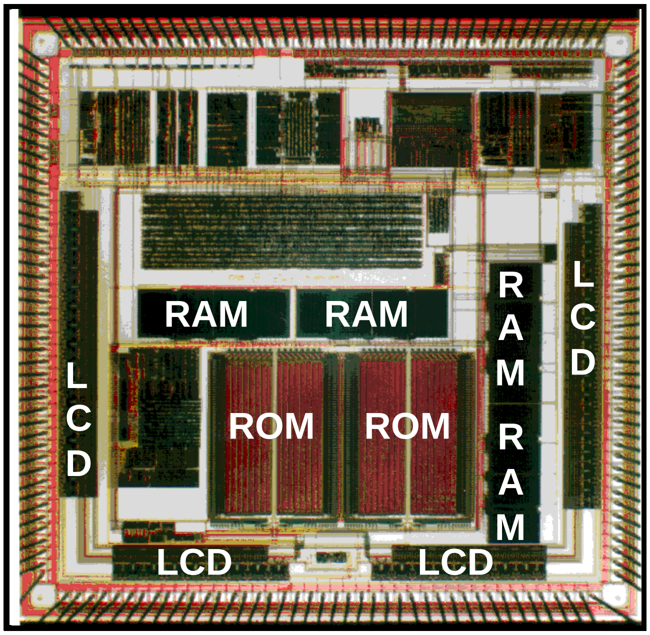


Figure 3. Modulated logic low for gate oxide stress relief of charge pump logic during start up.



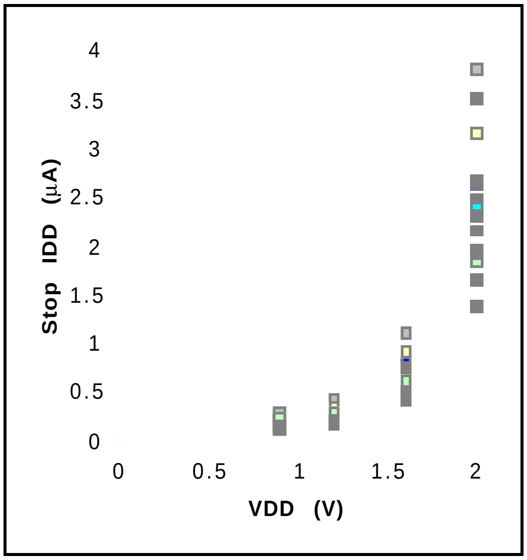
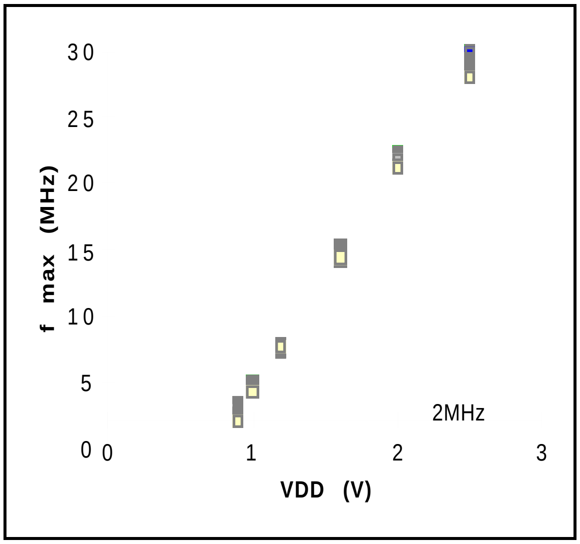


Figure 4. Microcontroller die photo

Figure 5. CPU stop Idd.



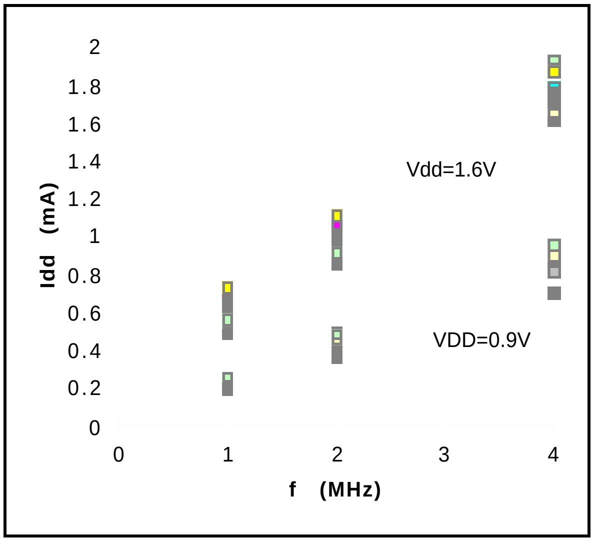


Figure 6. CPU maximum frequency.

Figure 7. CPU Run current at 0.9V and 1.6V.