

# Compact Modelling of Submicron CMOS

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## ABSTRACT

The accuracy of present-day compact MOS models and relevant benchmark criteria are reviewed. The impact on compact modelling of new CMOS applications and the rapid progress in process technology towards dimensions of 0.1 micron, will be discussed.

## 1 Introduction

In the computer-aided design of integrated circuits the compact model describes the device behaviour as a function of bias conditions and device geometry. Consequently this compact model is a critical link in the translation of CMOS process properties into IC performance. The application areas of CMOS technology are expanding and the CMOS process technology itself is making rapid progress towards dimensions of 0.1 micron. Moreover, the IC industry has recognised the need for a standardisation of compact models. This paper discusses the consequences of these developments for the field of compact modelling.

## 2 Accuracy and benchmark criteria

To benchmark the accuracy of compact models for digital applications it is sufficient to compare simulated and measured data for the linear current ( $V_{gs} = V_{supply}$ ;  $V_{ds} = 0.1V$ ) and the saturation current ( $V_{gs} = V_{ds} = V_{supply}$ ). In 1993 Tsvividis and Suyama published a number of qualitative benchmark tests for analog compact models [1, 2], while in the same year a new method for the evaluation of the accuracy of such compact models was introduced (see [3] and Table 3).

In the past years, within the IC industry the need for standardisation of compact models, being the interface between the design community and the IC foundries, has been recognised [4]. This has resulted in a series of workshops on compact modelling in the U.S.A., which was started by SEMATECH in March 1995. From discussions during the first two workshops a list of both qualitative and quantitative benchmark tests for dc and ac behaviour was compiled [5]. At the fourth workshop,

extensive comparisons of two selected public-domain compact models, BSIM3 [6] and MOS MODEL 9 [7], were presented [8, 9]. The results are summarised in Tables 1 and 2. In Table 3 the original data from [3] are reproduced together with data for BSIM3V2 on the same process [10]. Results for BSIM3V3 are expected to be slightly better.

From the data presented in Tables 1-3 it can be concluded that present-day compact models have reached an accuracy for the dc characteristics that is quite sufficient for most applications and hard to surpass. Until now only results on the qualitative ac benchmark tests have been become available. However, as will be discussed in the next section, the ac behaviour of compact models is of importance for new CMOS applications.

	n-channel			
	BSIM3V3		MM9	
$T$ [ $^{\circ}\text{C}$ ]	25	all	25	all
0.35 $\mu\text{m}$ process	2.6	4.0	3.0	5.5
0.8 $\mu\text{m}$ process	2.1	4.9	2.2	7.6

Table 1: Mean deviation (in %) between measured and simulated (using BSIM3V3 and MOS MODEL 9) characteristics for *i*) room temperature and *ii*) averaged over 3 temperatures (ranging from - 55  $^{\circ}\text{C}$  to 150  $^{\circ}\text{C}$ , indicated with “all”). Deviations are averaged

over linear, saturation and subthreshold region and output conductance and over 9 and 12 geometries for the 0.35  $\mu\text{m}$  and 0.8  $\mu\text{m}$  process, respectively (see [8]).

	n-channel						p-channel					
	BSIM3V3			MM9			BSIM3V3			MM9		
$T$ [ $^{\circ}\text{C}$ ]	27	85	125	27	85	125	27	85	125	27	85	125
$I_d - V_{gs}$	1.0	1.3	1.3	1.3	1.4	1.4	0.9	0.9	1.0	1.3	1.0	1.0
$I_d - V_{ds}$	2.3	2.8	2.9	3.7	3.5	3.3	1.7	2.3	2.8	3.8	3.8	3.7
$g_{ds} - V_{ds}$	16	16	17	13	11	14	10	13	16	18	18	19

Table 2: Mean deviation (in %) between measured and simulated (using BSIM3V3 and MOS MODEL 9) characteristics for *i*) 3 different temperatures and *ii*) three operating regions: linear region ( $I_d - V_{gs}$ ), saturation region ( $I_d - V_{ds}$ ) and output conductance ( $g_{ds} - V_{ds}$ ). Deviations are averaged over several bias conditions and over 10 geometries of an 0.5  $\mu\text{m}$  process (see [9]).

	n-channel		p-channel	
	BSIM3V2	MM9	BSIM3V2	MM9
$I_d - V_{gs}^a$	3.3	2.8	4.0	3.2
$I_d - V_{ds}$	8.2	5.9	8.0	5.4
$I_d - V_{gs}^b$	31	20	31	31
$g_{ds} - V_{ds}$	32	24	28	21
$I_b - V_{gs}$	72	26	84	27

Table 3: Mean absolute deviation (in %) between measured and simulated (using BSIM3V2 and MOS MODEL 9) characteristics. In addition to Table 2 also the deviations for subthreshold region ( $I_d - V_{gs}^b$ ) and substrate current ( $I_b - V_{gs}$ ) are

indicated. Deviations are averaged over several bias conditions and over 14 geometries of an 0.8  $\mu\text{m}$  process (see [3, 10]).

### 3 New applications

The rapidly decreasing minimum channel-lengths in CMOS processes lead to a drastical improvement of the high-frequency performance [11]-[14]. Moreover, this high-frequency performance can be combined with low noise figures and low power consumption [15]. Consequently, CMOS becomes more and more suited for RF and high-frequency applications.

As literature on high-frequency measurements of MOSFETs is scarce [16], the more so are publications on the comparison of these measurements with compact model calculations (see [14], [17] and Fig. 1, which was reproduced from [14]).

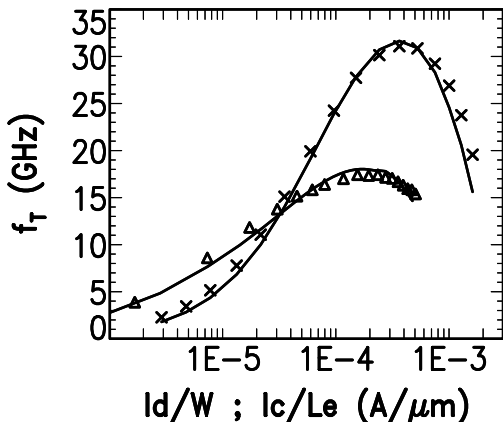


Figure 1: Unity current-gain frequency as a function of collector current per unit emitter length and drain current per unit gate width, respectively. Symbols indicate measurements: triangles  $0.5 \mu\text{m}$  n-channel MOSFET; crosses  $1 \mu\text{m}$  npn from a high-frequency bipolar double-poly process [18]. Lines indicate compact model simulations: MOS MODEL 9 for MOS and MEXTRAM for bipolar [19].

From the first comparisons of high-frequency measurements and compact model calculations (using MOS MODEL 9) it turns out that it is crucial to include a number of parasitics in the model calculations. Not only junction and overlap capacitances should be taken into account, but also the bulk resistance and especially the gate resistance. Taking these parasitics into account, both the bias and frequency dependence of a number of important quantities, such as impedance, transconductance, current and voltage gain, can be modelled with good accuracy [17].

## 4 Advanced process technologies

### 4.1 New physical phenomena

In Sect. 2 we have seen that present-day public-domain compact models describe the dc transistor characteristics of technologies with minimum dimensions down to  $0.35 \mu\text{m}$  accurately. However, it turns out that the same holds for processes with smaller dimensions [20, 21]. This is demonstrated in Fig. 2. Note that also the bulk current, which is generated by avalanche multiplication, is well-described. An explanation for these observations can be found by looking at the mobility reduction  $F(V_{\text{gs}}, V_{\text{ds}}, R_{\text{series}})$ , defined by

$$I_{\text{ds}} = \frac{\beta}{F(V_{\text{gs}}, V_{\text{ds}}, R_{\text{series}})} \left\{ (V_{\text{gs}} - V_{\text{T}}) V_{\text{ds}} - \left( \frac{1 + \delta}{2} \right) V_{\text{ds}}^2 \right\} . \quad (1)$$

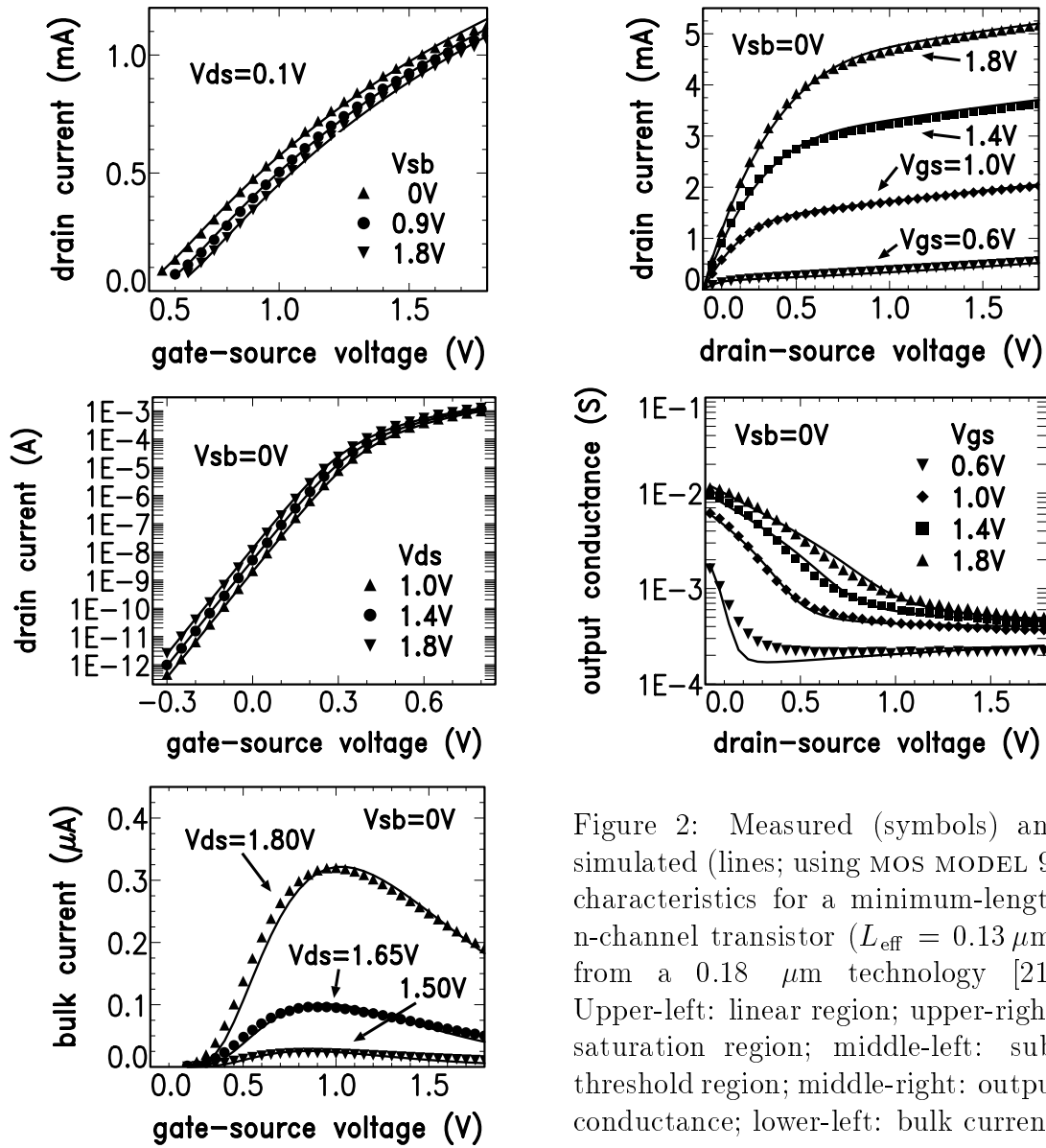


Figure 2: Measured (symbols) and simulated (lines; using MOS MODEL 9) characteristics for a minimum-length n-channel transistor ( $L_{\text{eff}} = 0.13 \mu\text{m}$ ) from a  $0.18 \mu\text{m}$  technology [21]. Upper-left: linear region; upper-right: saturation region; middle-left: sub-threshold region; middle-right: output conductance; lower-left: bulk current.

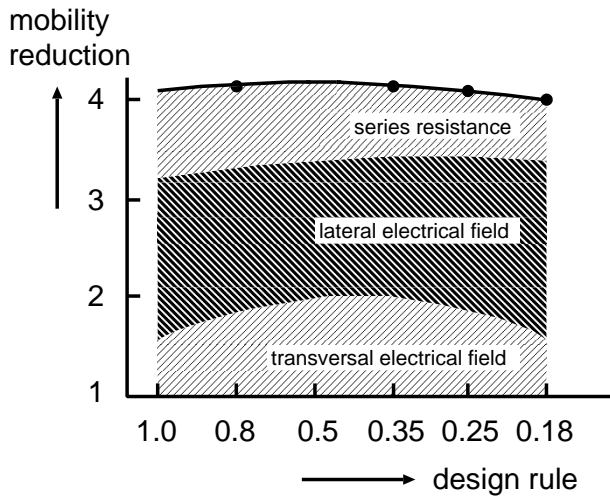


Figure 3: Mobility reduction  $F$  of the saturation current of minimum-length n-channel devices for various processes (see Eq. 1). The lower region indicates the contribution due to bias-enhanced surface scattering; the middle region indicates the contribution due to velocity saturation; the upper region indicates the apparent contribution due to the series resistance.

In Fig. 3 this mobility reduction  $F$  is shown for minimum-length devices from various processes in the saturation region ( $V_{gs} = V_{ds} = V_{supply}$ ). This figure shows that not only the reduction itself, but also the various contributions to this mobility reduction are almost constant. This implies that for an  $1.0\ \mu\text{m}$  process, velocity saturation is as important as it is for a  $0.18\ \mu\text{m}$  process. The need to take new physical phenomena, such as e.g. velocity overshoot, into account in compact modelling is not yet apparent.

## 4.2 Process control and parameter statistics

The supply voltage of the CMOS processes shown in Fig. 3 drops with decreasing minimum channel-length: from 5 V for the  $1.0$  and  $0.8\ \mu\text{m}$  processes, via 3.3 V for the  $0.5$  and  $0.35\ \mu\text{m}$  processes to 2.5 V for the  $0.25\ \mu\text{m}$  process and 1.8 V for the  $0.18\ \mu\text{m}$  process. This implies that the design window has been reduced considerably. Consequently, process control becomes a key issue.

The use of “direct” parameter extraction techniques [22, 23] instead of optimisation allows end-of-line compact model parameter determination. Direct parameter extraction facilitates process control in terms of compact model parameters and avoids cumbersome translation of conventional end-of-line electrical measurements into compact model parameters. Furthermore, direct parameter extraction enables the quantification of the matching performance [24]. Moreover, the availability of large data sets of compact model parameters allows the study and modelling of the correlation between these parameters [25]. This is of crucial importance to obtain a realistic design window.

As an illustration we show in Figs. 4 and 5 the parameter statistics of a batch with 3 different threshold-adjust implantations (identical for both n- and p-channels).

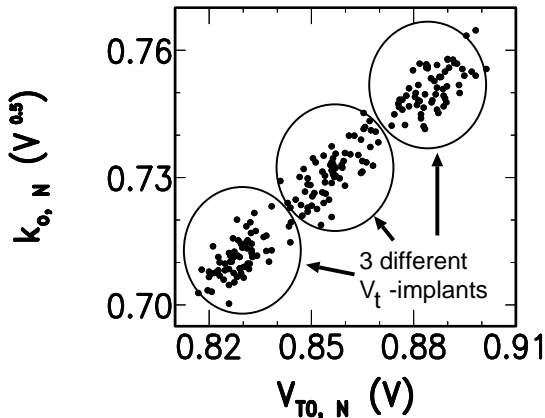


Figure 4: Body-effect factor,  $k_{0,N}$ , versus threshold voltage,  $V_{TO,N}$ , for two hundred n-channel transistors from a batch with three different implantations to adjust the threshold voltage.

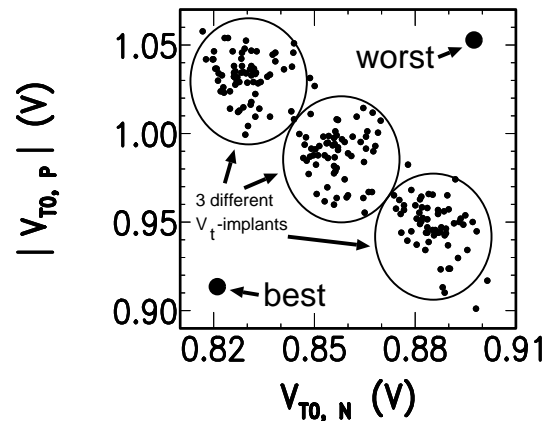


Figure 5: P-channel threshold voltage,  $V_{TO,P}$ , versus n-channel threshold voltage,  $V_{TO,N}$ , measured on 200 pairs from the same batch as Fig. 4. The conventional choice for best and worst case is also indicated.

From Fig. 4 it can be seen that the threshold-adjust implantation produces a correlation between body-effect factor and threshold voltage, which is similar to that produced by variations in oxide thickness. From Fig. 5, however, it shows that the threshold-adjust implantation produces a correlation between the threshold voltages of n- and p-channels, which is opposite to that produced by variations in oxide thickness. Consequently, the conventional worst-best case approach (based on variations in oxide thickness) would fail to reflect these variations in threshold-adjust implantation (as indicated in Fig. 5).

## 5 Conclusions

Present-day public-domain compact models describe the dc transistor characteristics of technologies with minimum dimensions down to  $0.35\ \mu\text{m}$  with an accuracy that is hard to surpass. The charge descriptions of these compact models have not been benchmarked as extensively as the descriptions for the currents. The first comparison of high-frequency measurements and model calculations, however, has shown no real deficiencies.

There are indications that the present-day compact models are also suited for processes down to  $0.18\ \mu\text{m}$ . The real challenge of these advanced CMOS processes lies in the statistical modelling which is to ensure that the designers are offered a realistic design window. The development of the parameter extraction methods and simulation tools needed for statistical modelling requires considerable effort.

These observations, in combination with the attempts to achieve a standardisation of compact models, leads to the expectation that the present-day public-domain compact models will be developed in an evolutionary way to cope with the requirements of future CMOS processes.

## 6 Acknowledgement

K.G. McCarthy of the NMRC, Cork, Ireland, is gratefully acknowledged for the BSIM3 data presented in Table 3.

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