40 GHz Narrow-Band Trans-impedance Trans-admittance Amplifier in InP-HBT Technology

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Abstract

A narrow-band amplifier with a center frequency of 40 GHz and bandwidth of approx. 600 MHz has been designed and fabricated in Hughes Research Laboratories' (HRL) InP-HBT technology. The amplifier operates between 3.3 and 4.0 V. At a center frequency of 40 GHz a current consumption of 26 mA (including the load) has been registered.

1.Introduction

In conjunction with the development of a 40 Gb/s demonstrator [1], the necessary circuits for an InP-HBT-based clock recovery structure has been implemented in the Hughes Research Laboratories (HRL) technology. The microwave filter based structure was made by MHSERC [2]. The necessary subcircuits have been implemented as separate blocks in order to simplify the evaluation during the first phase of the project i.e.verification of a fully electronic demonstrator based on hybrid mounted circuits. A monolithic integration of a complete receiver seems feasible using HBT-technology. This is very attractive when operating at extremely high clock rates, and especially when retrieving the clock through an asynchronous channel, because of the elimination of unnecessary HF I/Os. In the analog parts, circuit complexities have varied from 20 to 150 active devices.

2. Devices and Technology

HRL AlInAs/GaInAs single heterojunction bipolar transistor technology [3,4] offers more than 95 GHz f_T and 100 GHz f_{MAX} on the active devices, two layers of interconnect isolated by polyemide, MIM-capacitors and TaN-resistors with 50 ohms/sq. The MIM-capacitors are created by Metal1-Si_3N_4-Metal2, allowing 0.3 fF/μm^2. The level of the technology is currently in the upper MSI region. LSI-technology is expected to be available in the near future.

3. The Clock Recovery Structure

In order to clarify the target application for the amplifier, including the necessary specifications, a short description of the clock extraction principle is presented in Fig. 1. The respective system has the advantage of being independent of a Voltage Controlled Oscillator (VCO).

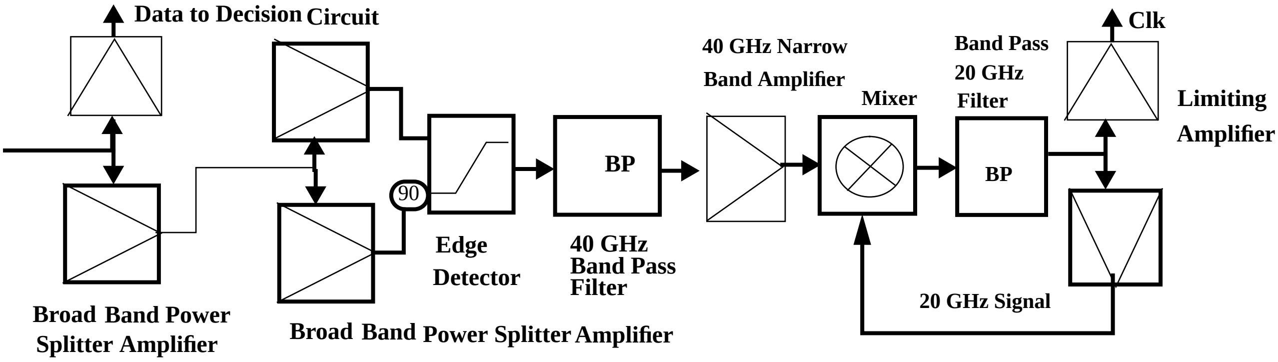

Figure 1. The Clock Recovery Circuit.

First the input signal is split and amplified. One branch is connected to the decision circuit, while the other is sent to another power splitter stage. One of the two outputs is shifted 90 degrees and thereafter both signals are fed to an edge detector. The 40 GHz component of the output is filtered with respect to phase and frequency through the bandpass filter and amplified by a narrow-band amplifier. The output locks the sub-harmonic oscillator to the phase of the input data.

The discrete band pass filters are connected to the circuit off-chip by wire bonding. The remaining active circuits implemented in the HRL technology are to be mounted on a carrier together with the 1:4 DEMUX circuit designed in the same technology.

4. The Narrow-Band Amplifier

In the narrow-band amplifier implementation, the trans-impedance trans-admittance amplifier structure was used according to Fig. 2. This feed-back amplifier is widely used for wide-band applications [5]. In this case, the narrow-band characteristics of the structure have been exploited utilizing delta-type inductors, prior to the output-pads, see Fig. 3. In order to remove any DC-off-set errors, the inputs were AC-coupled with 1pF capacitance. The main reason for the choice of amplifier structure has been the achieved tuning. The center frequency is created by tuning the resonance between the base-collector capacitance of Q and L. By varying the bias currents I1 and I2 of the amplifier the center-frequency may be changed as the base-collector capacitance of the transistors are bias-dependent, see Fig. 2. Thereby, a robust structure is encountered where narrow-band behaviour is achieved without the need for precise modelling of the inductors and transistors. Nine different versions of the amplifier were implemented. The difference between the amplifiers were mainly the inductors. By taking into account the dispersion and skin-effects, the inductors were designed between 100-200 pH assuming a 100 μm thinned substrate. The emitter area of Q was chosen in such a manner that the 40 GHz center frequency could be achieved even with unthinned substrate i.e. with 2 to 2.5 times larger inductor-values. The geometries were carefully layed out, considering the influence of the surroundings on the delta inductors. The T-structure at the output-pads gives rise to unwarranted effects which may be one of the mechanisms behind the phase behaviour, observed during the measurements, see Fig.4.

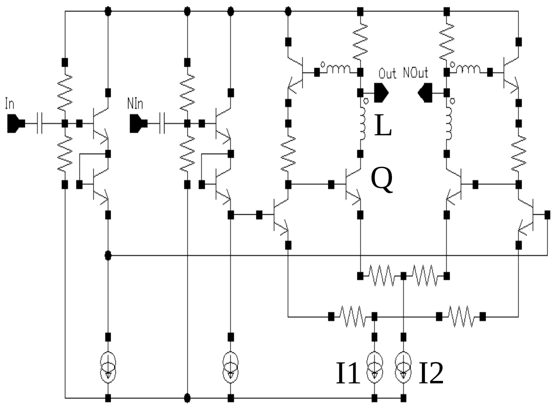

Figure 2. The Amplifier Schematic.

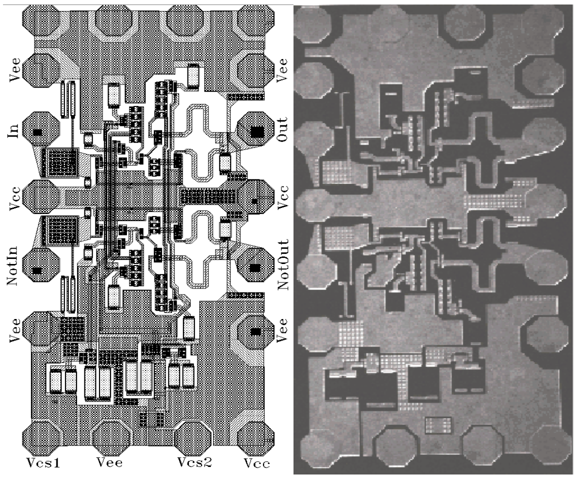

Figure 3. The Layout (left) and the SEM-Photo (right) of the Amplifier.

4. Measurements and Results

Using Wiltron 360 network analyzer, measurements were performed up to 50 GHz. It is important to point out that the 40 GHz power-signal-ground-signal-power wafer-probes, contribute to phase error both during the calibration, which is performed assuming an unbalanced amplifier, and when measuring above 40 GHz. The center frequency of the amplifiers varied between 37.5 GHz and 43 GHz, at power levels between -3.0 V and -3.3V, depending on the inductor values. Each amplifier showed tunebility within 1 to 1.5 GHz range. No signs of oscillation were detected when changing Vee down to approximately -4 V without input signal. At higher power levels, signs of oscillation were observed on the frequency response of the amplifier, but the actual oscillation frequency has not yet been determined. The 180-degree-phase shift at the resonance frequency is proper, although the phase shift turns unexpectedly just after the center frequency. The circuit

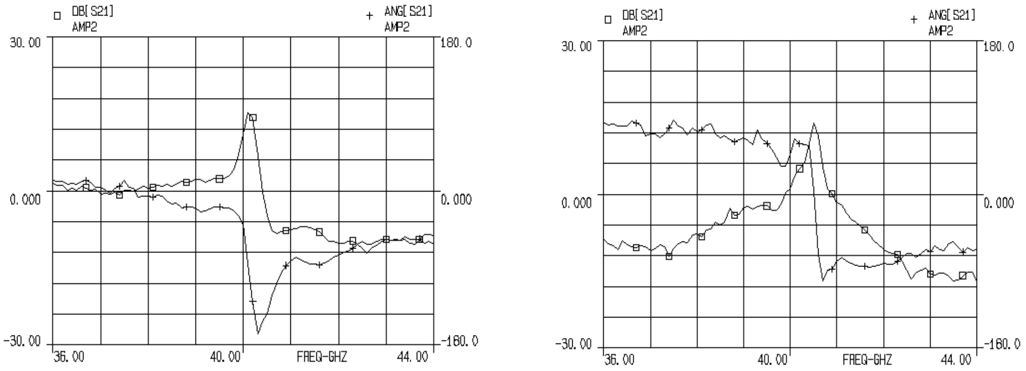

Figure 4. The Frequency Response of two Amplifiers with Different Inductor Values.

seems to have a combination of serial and parallel resonance, see Fig 4 (left). The behaviour may a. o. be due to geometry effects.

5. Acknowledgment

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