

A 50 MHz, standard CMOS, pulse equalizer for hard disk read channels.

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Abstract: A pulse equalizer for hard disk systems is presented. Opposed to classical realizations it is full CMOS while operating at 50 MHz cut-off frequency. For pulse slimming, the equalizer is capable of 13 dB selective boost around the cut-off frequency. The equalizer is a gm-C, seventh order 0.05° equiripple-on-the-phase low pass filter. It is made out of highly symmetrical biquads with elementary OTAs. The inaccuracies are compensated with a in this work introduced tuning system. This guarantees a ripple on the group delay of 2 %. The results are confirmed on silicon.

Introduction.

Pulse equalizers are found in all types of hard disk read channels. In peak detection based channels they act as pulse slimmers to reduce intersymbol interference. In PRML channels (partial response, maximal likelihood detection), they are part of the partial response equalization process. Pulse equalizers are higher order low pass filters. As such, they also suppress outband noise. For pulse slimming the low pass filter is expanded with a boost function. This consists of selective amplification of the signal frequencies around the cut-off frequency. [4]

The pulse equalizer presented here is realized in standard 0.7μ CMOS. It has a cut-off frequency of 50 MHz. It is part of a larger system aiming at CMOS only hard disk circuitry. This is motivated by the reduced cost of CMOS circuits compared to bipolar or BiCMOS alternatives. In earlier pulse equalizer designs, the bipolar transistors are mostly used to position the parasitic poles high enough on the frequency axis. [6] The reason for this is discussed below. In CMOS this is only possible at the expense of unacceptable amounts of power. In this paper novel circuitry to overcome this problem is presented.

The pulse equalizer.

The pulse equalizer presented here is a seventh order 0.05° equiripple-on-the-phase, low pass filter. It is capable of 0-13 dB boost of the signal frequencies around the filter's cut-off frequency. This boost is measured at the cut-off frequency, relative to the low frequency gain of the filter. The most important specification of the filter is the ripple on the group delay. It is defined as the maximum deviation of the group delay relative to its nominal value. The ripple on the group delay should be below 2%.

To realize this specification the biquads shown in fig. 1 are used. The equalizer is made out of three biquads and a single pole section. The single pole section is based on the same principles as the biquads. The integrating capacitors in the biquad are the sum of all parasitic capacitors at the corresponding node. It is important to note that explicit capacitors are added. This reduces the power consumption. Furthermore, at the given frequencies the parasitic capacitors cannot be

ignored anyhow. This is also the reason why dummies are added to the biquad to make it symmetrical with respect to the impedances connected to both integrating nodes. In that case both node capacitances are equal. This is the only way to control the time constants of the biquad accurately enough. Accurate absolute value control or accurate ratio control of capacitances made out of several parasitic capacitance proved not to be possible.

To keep the ripple on the group delay well below the specified value of 2%, all parasitic poles in the transfer function of the filter must be located above 300 MHz. In CMOS this will cost enormous amounts of power. Therefore the presence of parasitic poles is avoided. To do this, elementary OTAs, without any internal nodes are used, see fig. 1. Therefore the OTAs don't have any parasitic poles. Thus there are also no parasitic poles in the transfer function of the biquads. The problem with these OTAs is that their output impedance is quite low. These output impedances are part of the node conductance seen at the integrating nodes of the biquads. The problem of the low output impedance of the OTAs is solved in the tuning system by tuning the ratio of the node conductance to the transconductance in the biquad.

The boost function is realized by adding two zeros with opposite sign to the filter's transfer function. When the frequency of both zeros is exactly equal this does not alter the phase characteristic nor the ripple on the group delay of the filter. The zeros are added by injecting extra current into the integrating nodes of two filter sections at high frequencies. For this, boost sections, as shown in fig. 1, are put in parallel to the input OTA of two of the four filter sections. The sign of the injected current determines the sign of the zero.

To change the amount of boost the frequency of the zeros is varied by changing the bias current of the *-marked OTAs in fig. 1. Positive feedback is used to locate the parasitic poles of the boost section high enough on the frequency axis so that the ripple on the group delay is not affected. At the same time the zeros can be positioned low enough to realize a sufficient amount of boost. However, it is not possible, with reasonable amounts of power, to position the parasitic poles so high in frequency that they do not influence the position of the zeros. Furthermore this influence changes when the zero frequency is varied. Therefore when changing the frequency of the zeros, the bias current of the *-marked OTAs is changed with a different factor in both boost sections. This compensates the influence of the parasitic poles on the boost zeros.

In the described pulse equalizer, there is one source of ripple on the group delay degradation left: transistor mismatch. This mismatch is inversely proportional to the square root of the transistor area. Therefore, a mathematical model of the filter was drawn. By means of this model and extensive Monte Carlo analysis the minimal required area of the transistors has been determined.

The tuning systems.

To realize the ripple on the group delay specification two types of parameters must be tuned: the ratios of the natural frequencies of the filter sections and the quality factor of the biquads. These parameters must be tuned with an accuracy of 1 %. To realize sufficient accuracy of the cut-off frequency, the absolute value of one time constant in the filter must be tuned with an accuracy of 10 %. This can be done with a charge comparison based tuning system. [5]

An alternative strategy would be to tune the absolute value of all time constants. In that case, both the cut-off frequency and the ripple on the group delay of the filter are tuned. This requires tuning of the absolute values of the time constants with an accuracy of 1%. This is not possible with the described filter topology at the given frequencies.

The natural frequency of the sections depend on $\tau=C/g$ and gm/g . The quality factors depend only on gm/g . (gm is the transconductance in the biquad, g is the node conductance and C is the node capacitance.) Therefore, two types of tuning systems are implemented. The first type is

shown in fig. 2. The feedback loop in this system tunes the ratio gm/g to the ratio k of the reference voltages. This ratio can be accurately determined by on-chip resistors. The second type of tuning systems tunes the ratio τ_2/τ_1 for the different sections. Time constant τ_1 is the C/g ratio of the first section in the filter. This tuning is done for τ_2/τ_1 by the circuit shown in fig. 3. It operates by first charging a replica node of the biquad. Then this node is discharged. The integral of the "discharge voltage" that appears at this node is proportional to τ_1 . This voltage is multiplied by k_{12} sampled and compared to a voltage that is proportional to τ_1 . This voltage is determined in the same way. The feedback loop in the tuning system acts to make τ_2/τ_1 equal to k_{12} . The factor k_{12} is determined by an on-chip capacitor ratio. This can be accurately controlled.

Both tuning systems are expanded with an automatic offset calibration loop. For simplicity it is not shown in fig. 2. This loop automatically adjusts the offset of one of the subtractor OTAs so that the overall offset induced error is zero. This calibration process is independent from the tuning.

Results.

A test chip containing the seventh order pulse equalizer and the corresponding tuning systems, was realized in 0.7μ CMOS, see fig 4. The total area is 10 mm^2 . During the layout special care was taken to preserve the symmetry of the biquads. This is done by using a rail structure for the interconnections.

The circuit operates from a 5 V power supply. The measured group delay is shown in fig. 5. The measured ripple on the group delay is 1.8 %. The measured cut-off frequency is 47.8 MHz. The power consumption is only 140 mW.

Conclusion.

A new, full CMOS, alternative for hard disk pulse equalizers is presented. It is based on a symmetrical biquad with elementary OTAs. The inaccuracies due to these OTAs are compensated in a novel charge comparison based suite of tuning systems.

From the measurements of the test chip it can be concluded that the equalizer meets its specifications. These specifications are comparable to or better than earlier published pulse equalizers. [2], [3] This is certainly true when one takes into account that the other realizations are in BiCMOS or bipolar technologies.

References.

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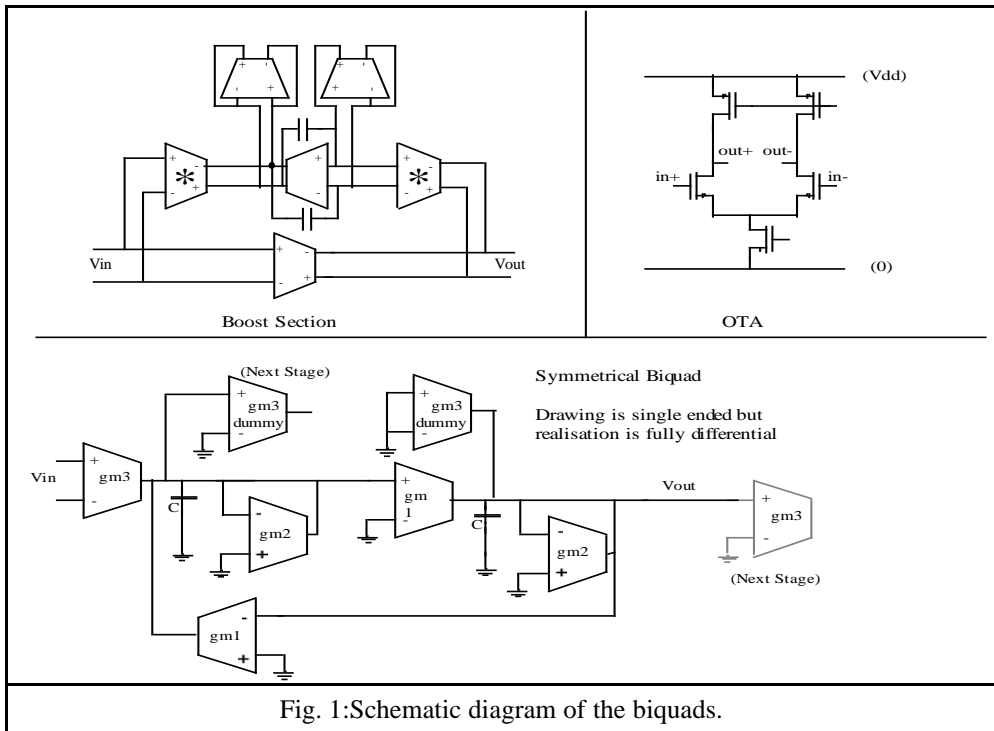


Fig. 1: Schematic diagram of the biquads.

