

# A FIELD PROGRAMMABLE ANALOG FUZZY PROCESSOR WITH ENHANCED TEMPERATURE PERFORMANCE

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## Abstract

*A field programmable analog fuzzy processor that supports 15 rules, three inputs and one output has been fabricated and tested. The chip area using a CMOS 0.7 $\mu$ m n-well technology is 32mm<sup>2</sup> with the analog core less than 7% of the total. Power consumption at 5V power supply is less than 45mW. The circuit functionality has been tested for power supply ranging from 4.75V to 5.25V and temperature in the interval between 0°C and 70°C. Applying a step input function, the output reaches a stable value in less than 0.6 $\mu$ sec.*

## 1 Introduction

In this paper we present a field programmable analog fuzzy processor designed using a CMOS 0.7 $\mu$ m n-well technology. The two main features of the chip, based on the analog core presented in [1], are that:

- the I/O relationship is insensitive over a wide temperature, power supply and process parameters range owing to a specific bias circuit requiring a single voltage reference;
- its architecture is clearly divided into an analog core and a digital part that supports the field programmability of the processor and relies on a software tool which computes the programming values to approximate a user defined I/O relationship [2]. This way the chip is very similar to an FPGA (Field Programmable Gate Array) since changing the contents of the RAM in the digital unit modifies the I/O relationship computed by the analog processor and allows fast system prototyping. Once the final configuration has been found, a dedicated minimum area system is automatically obtained simply substituting the RAM that stores the configuration with a ROM. Thanks to the complete separation of the digital and the analog units, the behavior of the programmable and dedicated processors is the same.

## 2 Processor Architecture and Circuit Design

A field programmable processor that supports 15 rules, 3 inputs and one output has been fabricated. The chip photo is shown in Figure 1 where three main units are recognizable:

- the analog processor unit and the I/O interfaces on the right side;
- the interface unit between an external EEPROM and the internal RAM via I<sup>2</sup>C protocol on the left;
- the digital programming unit which occupies the largest area in the middle.

### A. Analog Processor Unit

The modular architecture discussed in [1] has been implemented: each module corresponds to a rule and contains a number of blocks MF that generate trapezoidal Membership Function equal to the number of inputs ( $j = 1, \dots, n$ ), one Complement circuit and one operational transconductance amplifier (OTA).

The circuit diagram of the  $i$ -th rule ( $i = 1, 2, \dots, N$ ) is shown in Figure 2. The MF output current ( $\overline{I_{m_{ij}}(V_j)}$ ) [3] is the sum of the currents  $I_{sq_{1,2}}$  flowing through the two MOS differential pairs. Assuming all transistors in saturation region and neglecting drain current dependency on  $V_{ds}$ ,  $I_{sq}$  currents can be modeled as follows:

$$I_{sq} = \begin{cases} \frac{1}{2} \left( I_{gg} + K_f dV_{in} \sqrt{\frac{2I_{gg}}{K_f} - dV_{in}^2} \right) & \text{for } |dV_{in}| \leq \sqrt{\frac{I_{gg}}{K_f}} \\ 0 & \text{for } dV_{in} < -\sqrt{\frac{I_{gg}}{K_f}} \\ I_{gg} & \text{for } dV_{in} > \sqrt{\frac{I_{gg}}{K_f}} \end{cases} \quad (1)$$

where  $dV_{in} = V_{f_{ij}} - V_j$  is used when computing  $I_{sq_1}$  while  $dV_{in} = V_j - V_{r_{ij}}$  when computing  $I_{sq_2}$ .  $K = K' S$  where  $K' = \frac{\mu C_{ox}}{2}$  is the MOS transconductance parameter and  $S = (\frac{W}{L})$  its aspect ratio. The two programmable voltages  $V_{f_{ij}}$  and  $V_{r_{ij}}$  allow to set the position of the falling and rising slopes of the trapezoid.

The Complement circuit behaves like a half-wave current rectifier, computing the rule's truth-value current  $I_{g_i}$  as:

$$I_{g_i} = \max(0, I_{ref} - \sum_{j=1,3} \overline{I_{m_{ij}}}) \quad (2)$$

With reference to the simpler circuit discussed in [1], the proposed scheme has some major benefits: the feedback loop keeps voltage  $V_{m_i}$  constant acting as a regulated cascode for MOS transistor  $M_{ref}$  which generates current  $I_{ref}$ . In addition, the voltage  $V_{m_i}$  can be set to a rather high value ( $V_{m_i} = V_{dd} - V_{gs_{M_p}}$ ) by correct sizing  $M_p$  and  $M_n$ ; a wide dynamic range is therefore allowed on input voltages ( $V_j, V_{r_{ij}}, V_{f_{ij}}$ ) driving the MF circuits. The output value  $V_{out}$  is calculated using an approximation of the center of gravity (COG) method. The operational transconductance amplifier (OTA) acts as a two quadrant multiplier, one input being the current  $I_{g_i}$  and the other the difference  $C_i - V_{out}$ . Its output current can be expressed as:

$$I_{o_i} = \begin{cases} K_{ota} dV_i \sqrt{\frac{2\alpha_{mir} I_{g_i}}{K_{ota}} - dV_i^2} & \text{if } |dV_i| \leq \sqrt{\frac{\alpha_{mir} I_{g_i}}{K_{ota}}} \\ \alpha_{mir} I_{g_i} \text{sign}(dV_i) & \text{otherwise} \end{cases} \quad (3)$$

with  $dV_i = C_i - V_{out}$  and  $\alpha_{mir}$  the current mirror gain. Summing up the output currents of all OTAs on the high impedance output line, the DC output voltage satisfies condition  $I_{out} = \sum_{i=1}^N I_{o_i} = 0$  and is therefore the solution of equation:

$$\sum_{i \in I_{nonsat}} (dV_i) \sqrt{\frac{2\alpha_{mir} I_{g_i}}{K_{ota}} - (dV_i)^2} + \sum_{i \in I_{sat}} \frac{\alpha_{mir} I_{g_i}}{K_{ota}} \text{sign}(dV_i) = 0 \quad (4)$$

where the index  $I_{nonsat}$  defines rules with non-saturated OTA output current ( $I_{nonsat} = \{i : |dV_i| < \sqrt{\alpha_{mir} I_{g_i} / K_{ota}}\}$ ) while  $I_{sat}$  the ones with saturated OTA output current ( $I_{sat} = \{i : |dV_i| > \sqrt{\alpha_{mir} I_{g_i} / K_{ota}}\}$ ).

An out-of-range input or incomplete coverage of input domain would result in an indeterminate output value. To prevent this situation to occur, a special rule (called **ELSE**) is added in this chip. Its truth value can be set constant to a low degree of truth, independent of input voltages: its influence is therefore negligible during normal operation, when at least one rule is active, but its consequent determines the output value when the inputs configuration makes all rules inactive.

### B. Bias Circuits

The main improvement of the proposed chip is that the I/O relationship is made insensitive over a wide temperature, supply voltage and process parameter range thanks to a specific bias scheme featuring:

- all bias and programming voltages ( $C_i, V_{r_{ij}}, V_{f_{ij}}$ ) derived from a unique stable band-gap reference voltage ( $V_{BG}$ );
- the bias currents ( $I_{gg}$ ) of MF differential pairs proportional to the transconductance parameter  $K'$  but independent of threshold voltage  $V_t$ ;
- the reference current of the Complement circuit ( $I_{ref}$ ) proportional to the MF bias current.

Under these assumptions, from (1) and (2), we obtain that the current  $I_{g_i}$  is linearly dependent on  $K'$  but independent of  $V_t$ . The ratio  $I_{g_i} / K_{ota}$  therefore turns out to be insensitive to both parameters  $K'$  and  $V_t$  which are temperature and process sensitive. Only geometrical ratios, which can be very well controlled, and constant voltages appear therefore in (4) which determines the output voltage  $V_{out}$ .

In Figure 3 the bias circuit designed to meet the previous conditions is shown [4]. Defining  $A_n = S_{M2} / S_{M1}$  and  $A_p$  the mirror current gain, with  $A_p A_n < 1$  and assuming null output current, the loop forces:

$$I_{M1} = A_p I_{M2} \rightarrow V_{b0} = V_t + \frac{\sqrt{A_p A_n}}{1 - \sqrt{A_p A_n}} V_{BG} = V_t + \alpha V_{BG} \quad (5)$$

The voltage  $V_{b0}$  is used to bias the MF differential pairs, as shown in Figure 2: current  $I_{gg} = K' S_{gg} (V_{b0} - V_t)^2$  turns out to be equal to  $I_{gg} = K' S_{gg} (\alpha V_{BG})^2$ , hence independent of  $V_t$ , as required. The reference current  $I_{ref}$  of the Complement circuit is obtained from  $I_{gg}$  by means of a ratioed current mirror.

The floating voltage source shown in Figure 3(a) is obtained from the ground-referenced band-gap voltage  $V_{BG}$  thanks to the tunable level-shifter shown in Figure 3(b). The current conveyor (CCII-) forces the voltage  $V_x$  to be equal to the input voltage  $V_{BG}$  and the current flowing through transistor  $Md2$  to be equal to the one flowing

through  $Mu2$ . This current is mirrored in order to bias  $Md1$ : assuming  $Md1 = Md2$  the voltage drop between gate and source of  $Md1$  is  $V_{BG}$ .

### C. I/O Interface Circuits

In order to have the same  $0V - 2V$  range on both input and output variables, a level-shifting is performed. External input voltages are shifted-up to the internal  $V_j$  levels  $\in 1.8V - 3.8V$ , through a circuit based on the scheme shown in Figure 3(b) biased by one of the voltages generated by the resistor ladder. A level-shifter in the feedback path of the output buffer allows then to shift the internal output voltage ( $V_{out} \in 2V - 3.5V$ ) down to the external  $\in 0V - 2V$ .

### D. Digital Programming Unit

The I/O transfer function of the analog inference processor is programmed by means of the analog voltages  $V_{f_{ij}}$ ,  $V_{r_{ij}}$  and  $C_i$ . Four additional parameters are required to program the **ELSE** rule. The voltage levels are generated by a resistor ladder biased by the band-gap-referenced voltage  $V_{BG}$  as shown in Figure 4. The programming dynamic range is split in  $20mV$  steps equal to 1.33% of the internal output dynamic range. In the field programmable processor a digital bit-stream is serially loaded at power-up or by the activation of the **RESET** signal, to configure an internal switch matrix which connects the voltage levels  $V_a$  to the programming nodes  $V_{pr}$ . During the programming phase, the switch matrix is set to the correct state in order to synthesize a defined control function, while the analog output voltage is kept to ground. During processing operation, on the contrary, the digital logic is set to an idle state while the analog output voltage varies with analog inputs, following the programmed I/O characteristic.

Dedicated processors are readily obtained by hard-wiring the connections, and allowing to minimize the silicon area for a specific application. Since the analog processing unit is not modified, the I/O response does not change.

## 3 Measurements results

Table I summarizes the performance of the chip shown in Figure 1. Propagation delay is defined as the time for the output to reach the final value within a 1% of its full dynamic range when an input step is applied. It depends on the programmed target I/O relationship (i.e. on the number of active rules): a delay lower than  $0.6\mu sec$  was found for all the programmed functions. A dedicated processor featuring the same number of rules, inputs and output would occupy less than 7% of the total area of the field programmable chip.

As an example, in Figure 5 the measured DC response of the circuit programmed to approximate the *sine* function in the interval  $[-\frac{\pi}{2}, \frac{\pi}{2}]$ , normalized to the operating range  $0V - 2V$ , is plotted. When the input voltage  $V_{IN1}$  exceeds its valid dynamic range, the output value is set to  $1.5V$  by the consequent of the **ELSE** rule. The RMS and maximum errors between the measured characteristics and the expected ones are 1.2% and 2.6%, respectively, of the output dynamic range, while the maximum error with respect to the target *sine* function in its definition range is 3.2%. The spread between the 6 available chips is lower than 1%. Varying the supply voltage between  $4.75V$  to  $5.25V$  results in a maximum difference on measured characteristics of  $7mV$  equal to 0.35% of the output range. The difference between the output values measured at operating temperatures ranging from  $0^\circ C$  to  $70^\circ C$  and the corresponding values at  $28^\circ C$  is lower than  $22mV$ . This is partially due to the variation of the internal voltage reference  $V_{BG}$  (between  $1.281V$  and  $1.294V$  in the specified temperature range). When  $V_{BG}$  is forced by an external voltage source, the maximum difference decreases down to  $7mV$ . Comparable results are obtained by programming the chip to approximate different target functions.

## 5 Acknowledgments

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## References

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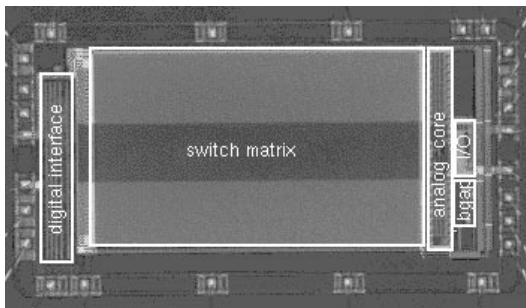


Figure 1. Chip Photo

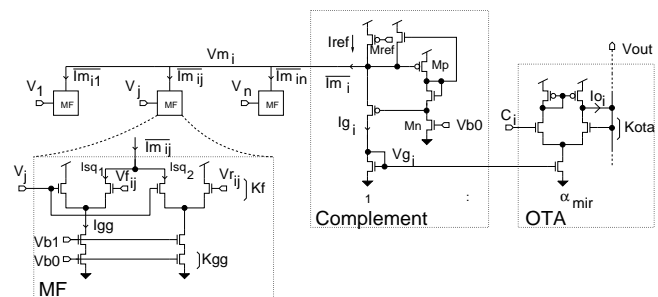


Figure 2. Circuit diagram of the generic rule

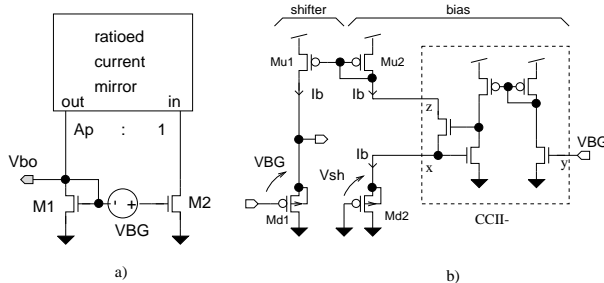


Figure 3. Circuit diagram of the bias circuit (a) and of the floating voltage source (b)

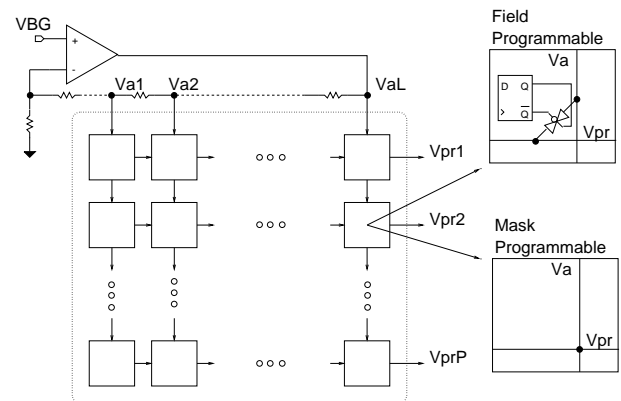


Figure 4. Digital Programming Unit

Table 1: Field Programmable Processor

Process	0.7 $\mu$ m CMOS
Number of Inputs	3
Number of Outputs	1
Number of Rules	15
Input Signal range	0 to 2V
Output Signal Range	0 to 2V
Supply Voltage	4.75 to 5.25V
Operating Temperature	0 to 70°C
Power Consumption	45mW
Analog core area	2.2mm <sup>2</sup>
Total area	32mm <sup>2</sup>
Propagation delay	0.6 $\mu$ sec

Table I. Chip Performance

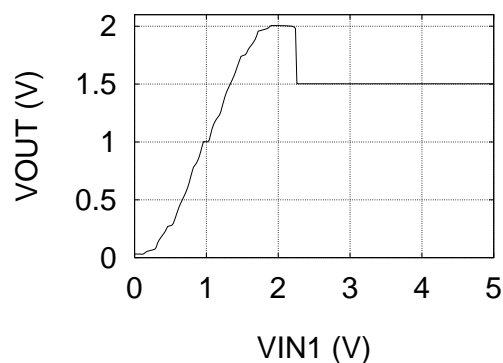


Figure 5. Measured characteristic when the chip is programmed to approximate the *sine* function