

A Low-Noise Low-Drift Transducer ADC

Damien McCartney, Adrian Sherry, Pat Hickey, John O'Dowd

Analog Devices, Limerick, Ireland.

Abstract

An ADC is described that achieves the very high resolution and low offset- and gain-drift required in converting the low-level output from a load-cell transducer. The ADC comprises a tare DAC, a PGA and a sigma-delta converter. The filter in the converter has a special mode to enable it to rapidly track changes in the transducer output. The ADC is also capable of accurately calibrating its gain in spite of the very small full-scale of 10mV.

Introduction

A signal-conditioning ADC has been developed to meet the very demanding resolution and drift requirements of the load cell transducer commonly used in weigh scales. An RMS noise of 50nV is required on the 10mV input signal with a bandwidth of 2Hz. The offset drift specification is 50nV/°C and the gain drift specification is 2ppm/°C. Figure 1 shows a block diagram of the converter. The signal conditioning includes a 2-channel fully differential multiplexer followed by a unity gain buffer. A 6-bit DAC allows removal of offset corresponding to the unloaded state of the load-cell. The offset-corrected signal is then applied to a programmable gain amplifier (PGA) before being input to a sigma-delta modulator for conversion. The PGA ranges of 80mV, 40mV, 20mV and 10mV are achieved by successively increasing the sampling rate of the modulator input capacitors by a factor of 2 [1].

Noise and Gain Drift

In the sigma-delta modulator the dominant sources of noise are quantization and thermal. Choosing a second-order modulator operating at 307.2kHz is sufficient to make the quantization noise insignificant. Thermal noise is determined by the size of sampling capacitor. Two 45pF capacitors are each sampled once on both phases of the modulator clock for the 80mV range; they are sampled 8 times per phase when operating on the 10mV range (i.e. at 4.9152MHz). Figure 3 illustrates 512 conversions on the 10mV range with a 2Hz bandwidth. The RMS noise is 31nV. With an 8Hz bandwidth (115ms settling time) the noise is typically 70nV, which is less than half that previously reported for such a converter [2]. The unity-gain buffer is employed to avoid loading the transducer bridge with the current drawn by these capacitors. The buffer is single-stage with a loop-gain greater than 100dB so that it does not contribute gain drift. Another potential cause of gain drift is mismatch between the 1pF modulator feedback capacitors and the 45pF input capacitors. Careful layout is employed.

Offset Drift

The components that will contribute offset drift are the buffer, the switches associated with the 45pF sampling capacitors and the first integrator amplifier of the sigma-delta modulator. Previously the buffer and integrator amplifier have both been chopped to remove their offset and 1/f noise [3]. This approach can achieve drifts of the order of 500nV/°C. In order to remove the contribution of the sampling switches the entire analog signal chain is additionally chopped. This is illustrated in Figure 2. The input is chopped before the buffer; the output chopping is done by inverting the bit-stream from the modulator. Figure 4 illustrates the improvement in drift from up to 500nV/°C to less than 20nV/°C when the additional chopping is enabled. The rate at which the input can be reversed is determined by the settling time of the Sinc³ filter [4] that follows the modulator. The default rate is 200Hz when the Sinc³ averaging factor is programmed to 512. This factor can be set as large as 2048. The chopping scheme is easily adapted to include the load-cell bridge as part of the chopped chain. A clock signal is provided to synchronize AC excitation of the load-cell and input chopping is not then required.

Filtering

Digital words are produced by the Sinc³ filter at the 200Hz rate and they include the input signal and the chopped offset. A 22-tap FIR filter performs the removal of the offset. It also sets the overall frequency response, achieving specified settling time and stop-band

attenuation. Figure 5 shows a plot of the frequency response with an averaging factor of 512. The bandwidth is 8Hz. It is 2Hz with the maximum averaging factor. This filter also has a special feature to enable it to respond rapidly to step inputs, for example when a weight is placed on the weigh-scale pan. The difference in successive words input to the filter is monitored and when it exceeds a threshold level the filter changes to performing an average of 2. The number of averages then increases to 4, to 8, to 16 and finally reverts to the full 22-tap convolution once 22 outputs have been processed after the step. The result is a rapid indication of the new value. Figure 6 illustrates the improvement in step response from 115ms to 15ms.

Calibration

A particular calibration challenge is that of gain calibration when the normal full-scale input is 10mV while the only calibration voltage available is the 5V reference. To attenuate the 5V reference very accurately for calibration the sampling capacitors are sub-divided into 32 smaller unit capacitors each of which is sampled in turn to get a charge corresponding to the average value of the unit capacitors. A further division of 16 is achieved by taking one sample per phase on alternative modulator cycles rather than 8 per phase on each cycle. The correction between the net attenuation of 512 and the desired attenuation of 500 is performed digitally.

General

The transducer ADC is fabricated on 0.6 μ m double-poly CMOS. There are 37k transistors on a die of 2.73mm X 4.35mm. The power supply is 5V and the supply current is 18mA.

References

- [1] McCartney, Damien, Welland, David R.: *Delta Sigma Modulator Having Programmable Gain/Attenuation*. US Patent 5,134,401, July 28th 1992.
- [2] Kerth, Donald A., Piasecki, Douglas S.: *An Oversampling Converter for Strain Gauge Transducers*. IEEE Journal of Solid-State Circuits, vol. 27, No. 12, pp. 1689-1696, December 1992.
- [3] O'Dowd, John, Hickey, Pat: *Data Conversion for Low Voltage Instrumentation*. Proceedings of Analog & Mixed Signal Design Conference, pp. P211-1 to P211-9, July 1994.
- [4] Candy, James C.: *Decimation for Sigma Delta Modulation*. IEEE Transactions on Communications, vol. COM-34, pp. 72-76, January 1986.

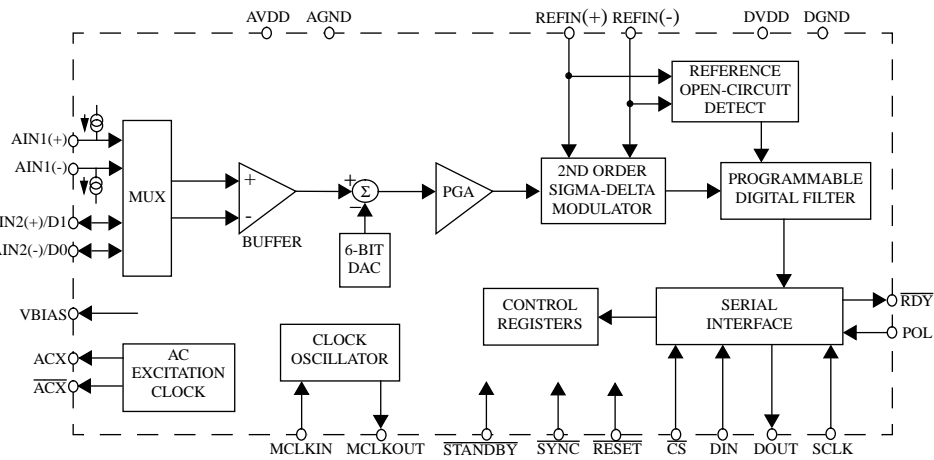


Figure 1: Transducer ADC Block Diagram

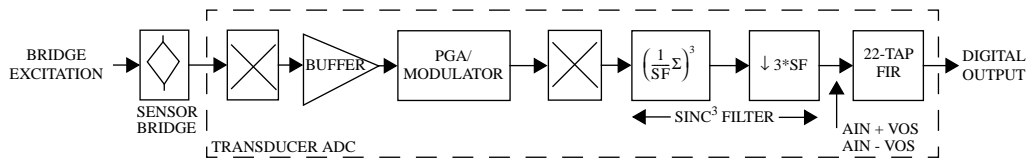


Figure 2: Chopping of Complete Analog Path

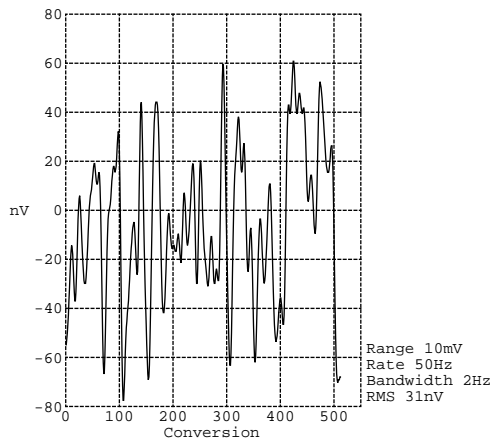


Figure 3: Measured Noise

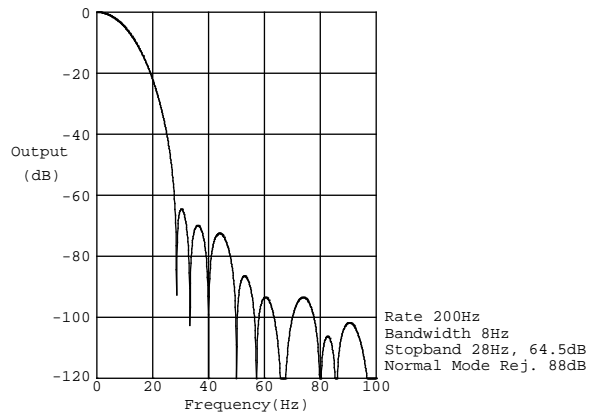


Figure 5: Frequency Response

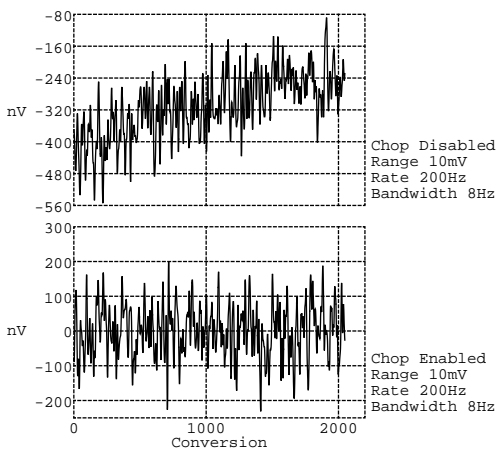


Figure 4: Measured Drift

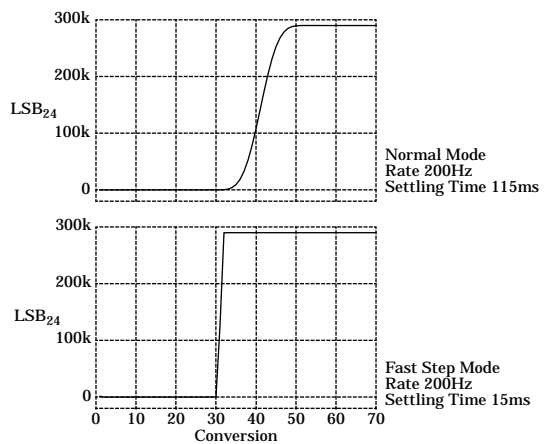


Figure 6: Fast Step Mode