

# **A 3.3V Power Adaptive 1244 / 622 / 155 MHz PLL**

D. BELOT, S.DEDIEU, L.DUGOUJON

SGS-THOMSON,  
850, Rue Jean Monnet BP 16 - 38921 Crolles, France

**ABSTRACT:** A power adaptive PLL for B-ISDN multi-rate [1] transmitter implementation in 0.5 $\mu$ m BiCMOS is described. The PLL power consumption matches the data rate by using a novel type ECL library. 210mW @ 155MHz to 320mW @ 1.2GHz total power is achieved. 17ps jitter at 1.2GHz is measured. Fast time to Silicon was performed by a Full Top-down design methodology.

## **1: INTRODUCTION**

This paper reports the design of a Phase Locked Loop (PLL) for on-chip bit serial clock generation inside high bit rates (155, 622, 1244 Mb/s) time division multiplexors.

Such a PLL is part of an ATM / SONET Line Termination monochip [2] [3] being designed in a 0.5 $\mu$ m BiCMOS process. To provide a cost-effective solution, special effort must be paid in cutting down the Power consumption according to the working bit rate. The challenge of this PLL design consists in the combination of low voltage supply (3.3V), power adaptive properties, high frequency (up to 1.25GHz), and low jitter.

## **2: CIRCUIT DESCRIPTION**

The PLL architecture is shown in figure 1, it is composed by a 1.25GHz VCO and a specific divider which supplies 155, 622 and 38.8 MHz frequencies. Bit rate choice (155, 622, 1244 MHz) is achieved by the selector blocks, another selector permits to replace the internal clock (CKI) with an external one for test purposes (CKE). A by 16 synchronous divider generates each subdivided frequency from CKI divided by 2 to CKI divided by 16. This lowest clock signal is compared in term of Phase and Frequency by PFC block to the parallel word input clock (CKW). The differential error outputs of PFC are then filtered by a low-pass filter and control back the VCO frequency. In case of non locked condition, an alarm signal is generated from a frequency comparator (LSCGcomp) connected to CKI divided by 8 and to CKW clock signals.



tors are sized for matching purpose. Double-base transistors are used to minimize base thermal noise which is the main contributor to the high frequency jitter. The voltage swing is 400mVpp differential which provides a good noise margin. To increase further the noise immunity of the PLL we have decided to design a full differential control loop (fig 5).

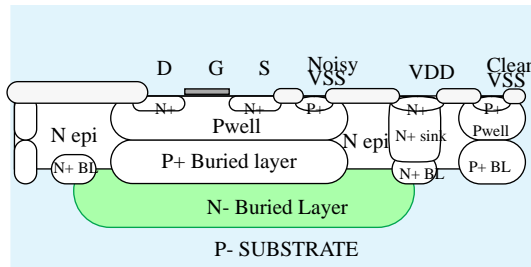


fig 4: Isolation

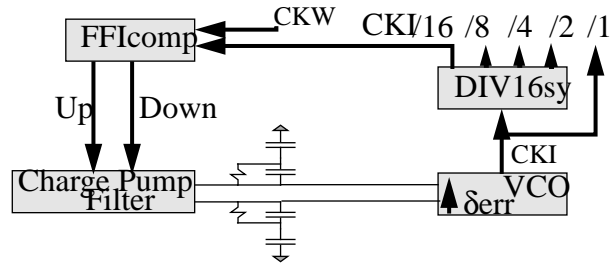


fig 5: Differential loop back

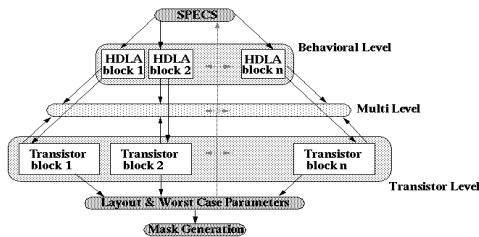


fig 6: Analog top down approach

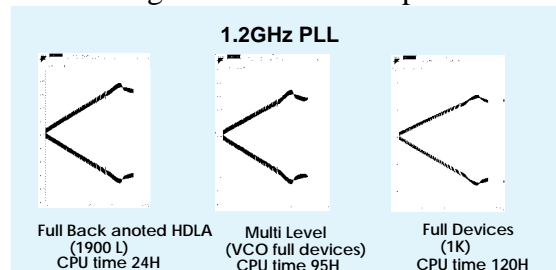


fig 7: Analog simulations

## 5: DESIGN FOR TESTABILITY

Testability issues were addressed with the goal of performing full frequency test of the PLL at the wafer level. Enabling controls of all high speed outputs have been implemented, the 1.244GHz rate is tested using the by 16 divided (80MHz) output, the other ones being disabled. To allow the Phase Frequency detector test, an external clock can be substituted to the internal one, making possible to measure the transfer function by probing the filter output. The VCO gain characterization is obtained by forcing the error voltage.

## 6: DESIGN METHODOLOGY

To perform faster time to market, a top down approach was endorsed [5] using a HDL analog language as it is described in the figure 6. First of all, starting from the PLL specifications we have defined the architecture, thus we have written the HDL models of the blocks to perform a system simulation. From this one we have defined the cells specs and transistor level cells are built to address those specs. Refinement of HDL cells models is achieved against (tr. level) simulation. Finally a multi-level simulation of the real cell (tr. level) connected to its environment (HDL cells) is done. Figure 7 shows a comparison between three simulations of the locking process of the PLL: a full HDLA, a mixed HDLA-tr., and a transistor one. The results fit very well (1%) and the HDLA simulation duration is a fifth of the transistor simulation one.

## 7: MEASUREMENTS:

(See PLL micrograph, figure 8). The PLL has been measured at wafer level. Figure 9 shows jitter measurement on packaged sample, the jitter standard deviation at 1.244GHz is equal to 17.7ps with 6us accumulation time, this figure is 19ps at 622MHz in same conditions. These measurements have been performed at 3.3V and 25<sup>0</sup>C.

Figure 10 shows the lock process of the PLL at 155Mbps data rate, in 54 $\mu$ s.

Table 1: PLL Main measurements results

PARAMETERS	25 <sup>o</sup> C			125 <sup>o</sup> C
	3.0V	3.3V	3.6V	3.3V
Free running frequency (MHz)	1385	1399	1412	1321
Max lock frequency in 155 MHz mode (MHz)	188	190	192	175
PLL power in 155 MHz mode (mW)	180	212	245	248
PLL power in 622 MHz mode (mW)		298		
PLL power in 1244 MHz mode (mW)		316		
Power down consumption (mW)	57	69	94	124
Lock process time in 155MHz mode (us)		55		
Measured Jitter in 622MHz mode (ps)		19		
Measured Jitter in 1244MHz mode (ps)		17.7		

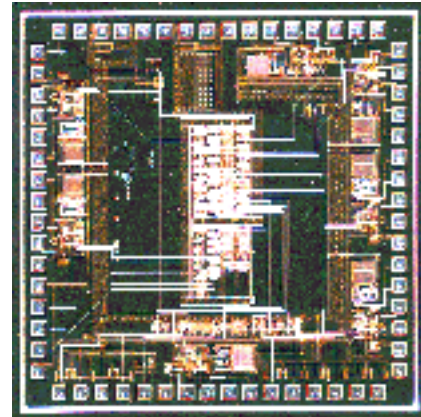


fig 8: PLL photo

Free running frequency exhibits 32ppm/mV sensitivity to power supply variation. The variation versus temperature is 557ppm/<sup>o</sup>C which doesn't affect the PLL due to the frequency margin. The VCO (not programmable CML) is always running to reduce lock time process. The jitter at low frequency is equivalent to 2% of period instead of 10% specified in ITU-I 432 [1].

### 8: CONCLUSIONS:

This Power adaptive PLL worked satisfactorily at the first cut, packaged in a 64 CQFP, it has been designed in 0.5um BiCMOS, offers low power and low noise features based on a combination of Bipolar and CMOS advantages. The power reduces from 316 mW at 1.244GHz to 212 mW at 155MHz which is very competitive. The jitter is lower than 20ps summarizing the strong effort in low noise design. The top down approach reducing the design time was applied with success in this work.

### REFERENCES:

- [1] ITU-I Recommendations I.432. B-ISDN User Network Interface - Physical Layer Specification (Mar.93).
- [2] "A 622 Mp/s line terminator for ATM network", ISSCC Digest of technical papers (Feb.93). M.Diaz Nava, J.Bulone, D.Belot, L.Dugoujon.
- [3] A 622/155 Mbps ATM Line Terminator Mono-chip ETC Digest of technical papers (Mar.95). M.Diaz Nava, D.Belot, P.Delerue, J.Bulone.
- [4] Patent 95/02840: "Circuit logique à étage différentiel" "Brevet d'invention"(Mar.95). D.Belot L.Dugoujon
- [5] "A practical approach to top down Analog circuit design" Proceedings ESSIRC'93 JP.Morin, F.Lemery, E.Necessian, V.Sharma, J.Benkoski, D.Samani

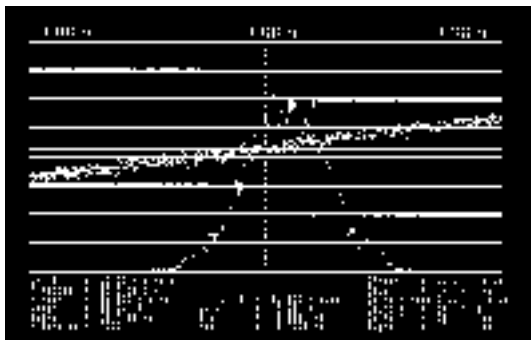


fig 9: Jitter measurement

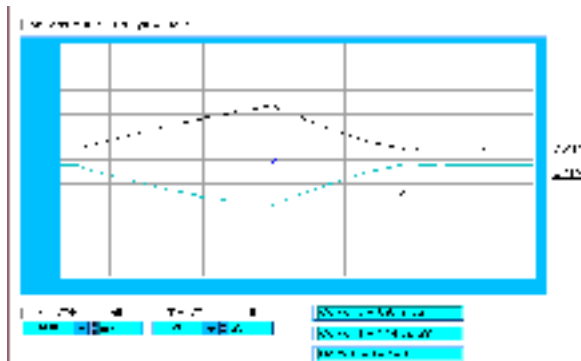


fig 10: Lock process