

A Multi-Level QAM Demodulator LSI with Wideband Carrier Recovery and Dual Equalizing Mode

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Abstract -- A 4-/16-/64-/256-QAM demodulator LSI with an all-digital carrier-recovery loop including a novel phase detector and a fractionally-/symbol-spaced equalizer is described. The phase detector, deciding the transmitted symbol from received signal power, detects the phase error up to +/-45 degrees and enables the loop to internally eliminate the +/-80 KHz carrier-frequency offset. The fractionally-spaced equalizer is implemented at the same clock rate as the symbol-spaced equalizer by only increasing the selectors and flip-flops, though the former theoretically requires a two times faster operation than the latter. An LSI operating at a symbol rate up to 8 MBaud is successfully implemented.

1. Introduction

Digital cable services such as interactive TV and modem systems are now ready for launch. The quadrature amplitude modulation (QAM) technique is a established modulation scheme for these services because of its high bandwidth efficiency [1]. QAM demodulator LSIs are desired so as to realize low-cost cable systems [2-4]. For robust cable systems, the following two QAM demodulator LSI functions must be improved. One is to eliminate the carrier-frequency offset mainly due to the inaccuracy of analog front-end circuits such as a tuner. The other is to equalize multi-path distortion caused by reflections in the cable channel.

This paper presents a 4-/16-/64-/256-QAM demodulator LSI with an all-digital carrier-recovery loop including a novel phase detector and a fractionally($T/2$)-/symbol(T)-spaced equalizer. The LSI eliminates a carrier-frequency offset up to +/-80 KHz in an 8-MHz bandwidth, while conventional LSIs empirically eliminate an offset less than +/-10 KHz. The advance lies in a newly-developed phase detector which detects phase errors up to +/-45 degrees. The $T/2$ -spaced mode is supported in the LSI as well as the conventional T -spaced mode, without increasing the clock rate. The $T/2$ -spaced mode operation is achieved by adding selectors and negative edge triggered flip-flops to the T -spaced circuitry. The two modes are controlled via a serial-bus interface. A software verification strategy results in a very high degree of design certainty, so that the complete functionality of the LSI can be guaranteed.

2. System Description

Figure 1 shows a block diagram of the QAM demodulator LSI. The chip has two carrier-

recovery circuits and a decision-feedback equalizer (DFE). The auto frequency control (AFC) loop and the auto phase control (APC) loop construct the outer and inner carrier-recovery circuits respectively. The AFC loop-filter output is fed back to the analog tuner to coarsely eliminate the carrier-frequency offset. The internally-closed APC loop removes the remaining frequency offset and phase jitter.

3. Wideband Carrier Recovery

As the AFC loop does not finely eliminate the carrier-frequency offset, the APC loop has an important role in carrier recovery. The novel phase detector, which detects a phase error up to ± 45 degrees, is the key component of the APC loop.

A block diagram of the phase detector is shown in Figure 2. First, transmitted symbols having similar power to the received signal (X_i , X_q) are predicted. Maximally four symbols (S_1 to S_4) are predicted for every received signal in the case of the 256 QAM. Then tangents of the phase error θ between the received signal and the predicted symbols are calculated (E_1 to E_4). The absolute values of the tangents are limited to less than 1. Thus, the detectable range of θ is bounded to ± 45 degrees. Each calculated error is assigned to one of 16 regions. A phase error is detected when the same region is assigned by four consecutively received signals.

In conventional phase detection the transmitted symbol is determined as that nearest to the received signal, as shown in Figure 3a. Thus, the detectable phase-error range depends on the QAM level. The range is as small as 7.7 degrees for 64 QAM or 3.4 degrees for 256 QAM. The proposed phase detector does not depend on the QAM level, because it uses the received signal power as shown Figure 3b.

The detectable phase range decisively influences the APC-loop performance. The boundary of the pull-in range of the present APC loop is up to ± 80 KHz, while it is empirically less than ± 10 KHz using conventional circuits.

4. Dual Equalizing Mode

The DFE has 8 feedforward taps and 16 feedback taps, where $T/2$ -spaced mode is applied to the feedforward taps. The $T/2$ -spaced equalizer performs better than the T -spaced one because of its wide bandwidth [5]. Some previous equalizer LSIs [3,4], however, do not support $T/2$ -spaced mode because the mode theoretically requires circuits operating twice as fast as those of the T -spaced mode.

Figure 4 shows a block diagram of the present equalizer. In $T/2$ -spaced mode, every other input data are loaded to the even-tap circuit at the positive clock edge. The remaining data is loaded to the odd-tap circuit at the negative clock edge. Each circuit acquires the data at half the rate of the input data, therefore the $T/2$ -spaced mode equalizer operates at the same clock rate as the T -spaced mode equalizer. The two modes are controlled via a serial-bus interface.

5. Results

A Signal Processing Worksystem (SPW;TM) hardware design model was used to verify the LSI functions. The pull-in time of the APC loop is shown Figure 5. In the cases of 10 KHz and 80 KHz the carrier-frequency offset errors are eliminated in 7 msec and 64 msec respectively. Figure 6 shows the I-phase output signal, Q-phase output signal, and APC loop-filter output. A breadboard was fabricated based on the hardware design model and its real time function was successfully confirmed.

Figure 7 shows a layout of the QAM demodulator LSI. The chip integrates 880,000 transistors in a die size of (12.87 mm*12.49 mm) using 0.5 micron CMOS 3-metal technology. The supply voltage is 3.3V. The LSI is packed in a 128-pin QFP.

6. Conclusions

A multi-level QAM demodulator LSI with wideband carrier recovery and dual equalizing mode was presented. The chip has a novel phase detector circuit that uses the received signal power. The signal which has a +/-80 KHz carrier-frequency offset is fully recovered in 64 msec. The T/2-spaced mode is supported in the LSI as well as the conventional T-spaced mode without increasing the clock rate. The T/2-spaced equalizing mode is achieved by adding selectors and negative edge triggered flip-flops to the T-spaced circuitry. The techniques of the QAM demodulator LSI presented will decrease the cost of digital transmission systems.

References

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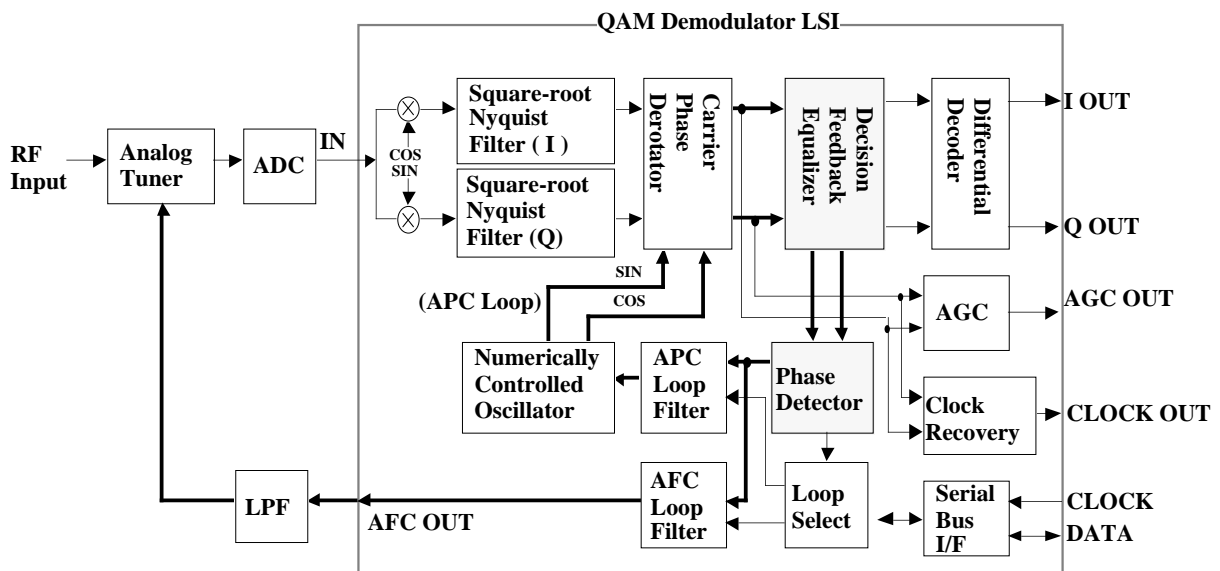


Figure 1. Block diagram of QAM Demodulator LSI.

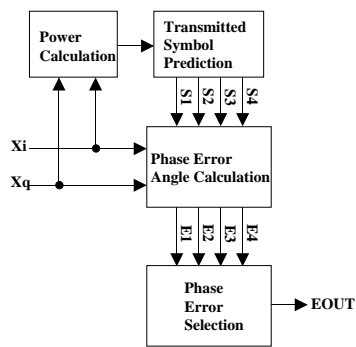


Figure 2. Block diagram of Present Phase Detector.

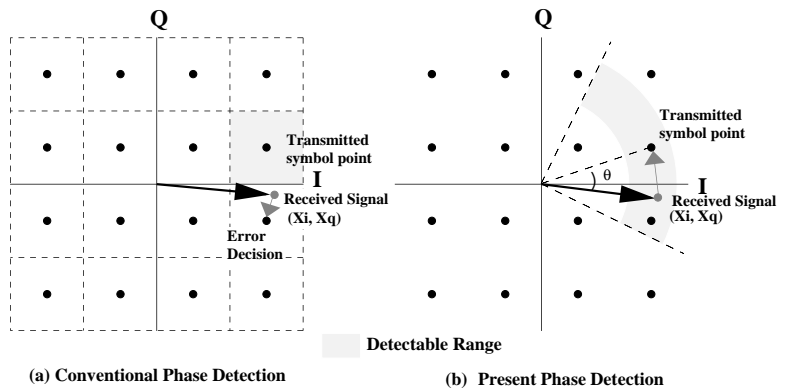


Figure 3. Comparison of Phase Detection (16 QAM).

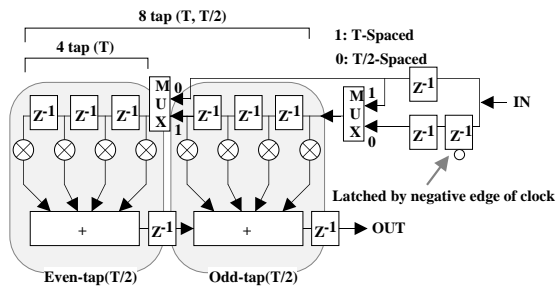


Figure 4. Block diagram of Present Equalizer.

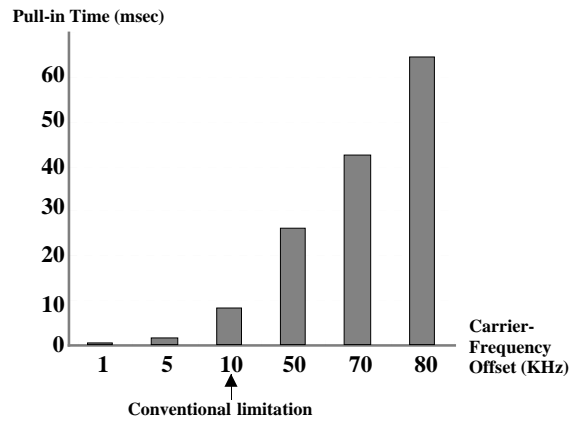


Figure 5. Pull-in Time of the APC Loop (64 QAM).

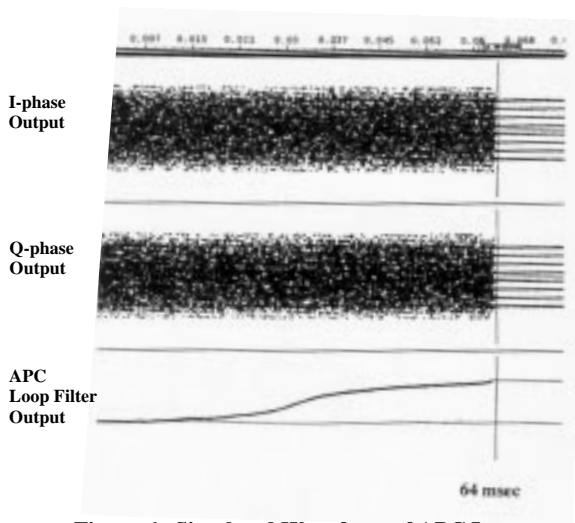


Figure 6. Simulated Waveform of APC Loop (64 QAM, Carrier-Frequency Offset = 80 KHz).

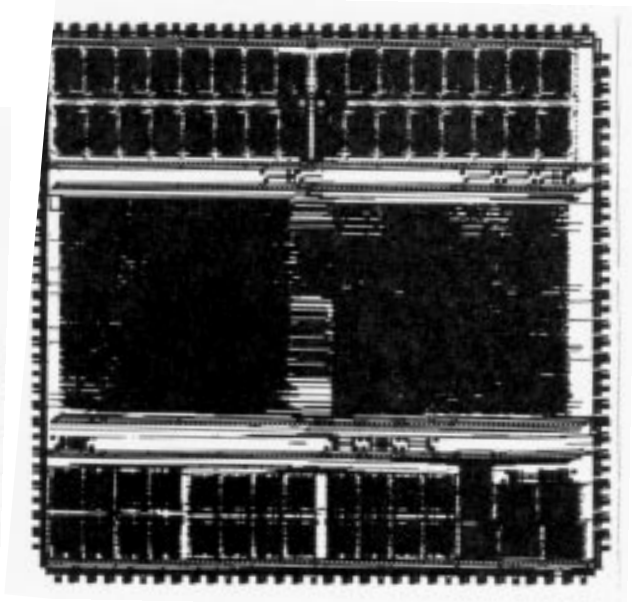


Figure 7. Layout of the QAM Demodulator LSI.