

# A 100Mb/sec. Multi-LAN Crosspoint Chip Set For Cable Management

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**Abstract:** A multi-LAN, 0dB insertion loss, analogue crosspoint switch chip-set is described which forms the heart of a new LAN cable management product [1]. The chip-set is capable of switching FDDI (TP-PMD), Ethernet, Token Ring and Half-Duplex protocols through a matrix of 108 x 108 cross-connects for services using 100m of unshielded twisted pair cabling and data rates of up to 100Mb/s using commercial CMOS and BiCMOS technologies.

## 1. Introduction

The multitude of different LAN standards installed by organizations has resulted in many problems for the user in terms of cable management [1] and LAN interoperability [2]. To address these problems an analogue crosspoint chip set has been developed to enable administration of multi-LAN network cabling. Analogue crosspoint switches (XPS) compete in performance in terms of matrix size, bandwidth [3] and switch resistance. Within a particular technology, any increase in performance of one of these parameters will result in the necessary degradation of the other parameters. To maintain non-blocking operation, passive XPS have been used which introduce a significant insertion loss due to the switch resistance, hence reducing the distance a signal may travel over a terminated cable medium. The design of a 0dB insertion loss multi-LAN XPS must take the above into account and also accommodate all the AC and DC signal requirements (Table 1) within a commercially attractive process.

In order to use a low voltage (i.e. low cost process) switch configuration an AC interface to the twisted pair cables was implemented to remove the high common mode (CM) voltages present during Token Ring operation. Also, to provide a reasonably large crosspoint ASIC switch (36x36 differential input/output) at low cost, a high switch resistance is necessary to minimize die area. The resulting design challenges to achieve a 100Mb/s, 0dB insertion loss switch for multi-LAN operation were:

1/ The ASIC ports interfacing to the LAN RJ45 cabling connector have to be able to accommodate transmit (Tx) or receive (Rx) operation depending on the particular LAN service and for Rx operation the input must be terminated.

2/ Achieving a high bandwidth for large ASIC switch configurations. Also, different signal paths will experience different bandwidths due to large changes of switch resistance ( $R_{on}$  with process batch and  $R_{metal}$  with ASIC signal path through the matrix).

3/ Amplification to make up the insertion loss due to the high switch resistance. Unfortunately the use of amplifiers block half-duplex LAN standards.

4/ The use of AC coupling blocks common mode (CM) voltage signalling necessary for Token Ring cable fault detection operation.

**2. Chip Architecture:** The architecture adopted uses a two ASIC solution (Figure 2); a Bi-CMOS Concentrator ASIC, which has two modes of operation, and a CMOS Crosspoint ASIC. The Concentrator ASIC, Table 2 and Figure 1, is the interface to the unshielded twisted pair (UTP) cable, taking four differential pairs from each LAN workstation user and concentrating them into one active differential Tx and Rx pair for communication to and from the Crosspoint ASIC. It also provides the interface to the LAN Hub, taking one differential Tx and Rx pair per user from the Hub and passing these pairs to the XP ASIC. The signal path that each user operates is determined by the LAN pair assignment being used on the station and Hub ASICs.

**3. The Concentrator ASIC:** This ASIC accommodates six users, each with four differential UTP ports and two differential XPS ports. Each user has a transmit path consisting of a 0 to -9dB attenuator; a 0 to +9dB differential current mode amplifier; and in the receive path a +15dB to +30dB differential current mode amplifier - see figure 2. All termination, gain and attenuator settings are programmable by writing to a RAM control area via a serial interface.

In order to achieve a return loss of -15dB the UTP ports, when configured as inputs, must be accurately terminated to <5%. Switchable on-chip terminations have been achieved using the circuit concepts shown in figures 3,4. A high gain amplifier ensures that the gate bias voltage on the FET switch produces an  $R_{on}$  equal to the external resistor - this voltage is then used to bias all terminations in the ASIC, variations due to processing & temperature will be accommodated by a change in the generated gate bias voltage. Figure 4 shows the switched termination; composed of a PFET/NFET combination and a 25 ohm series resistor which is used to improve linearity of the termination from 2% to 0.34% THD @ 5.6Vp-p differential. The ASIC achieves a differential termination matching of ~2% and absolute matching to the external reference resistor of typically 3% across the die. When the UTP is Tx (output) configured the termination is switched out in order to save power.

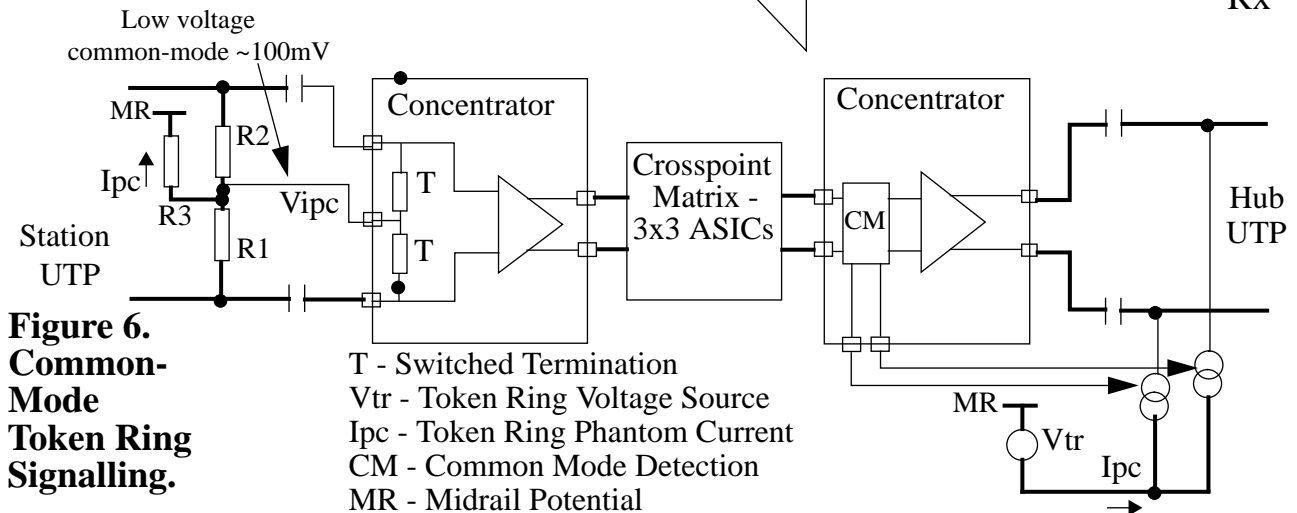
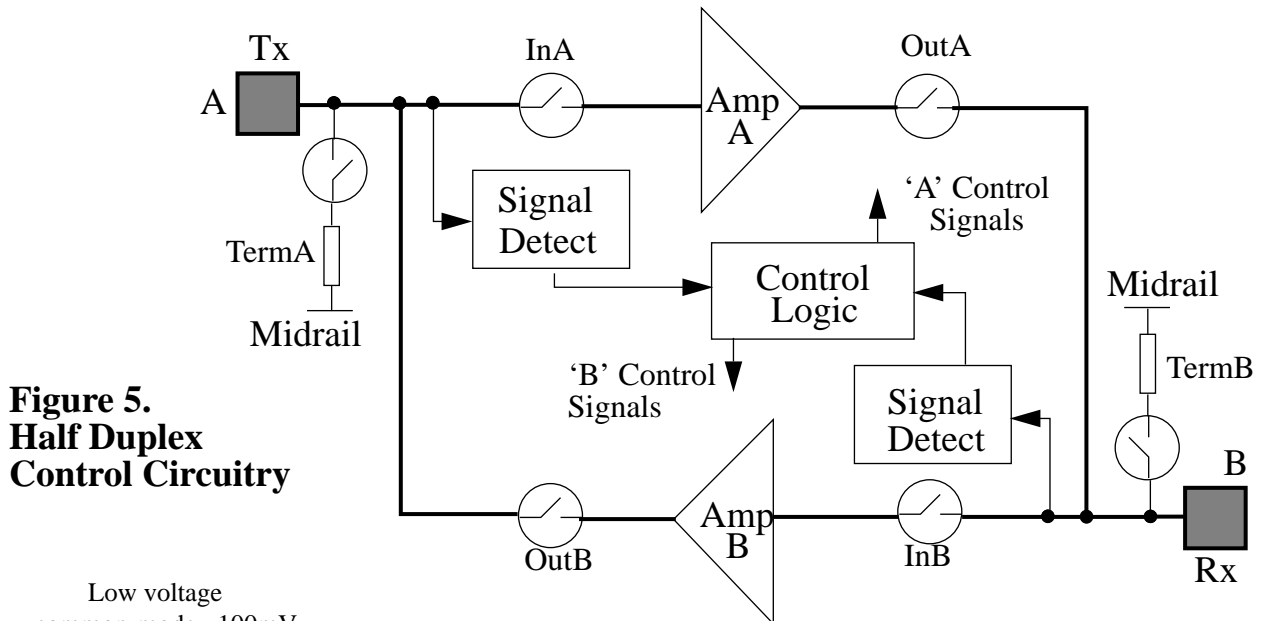
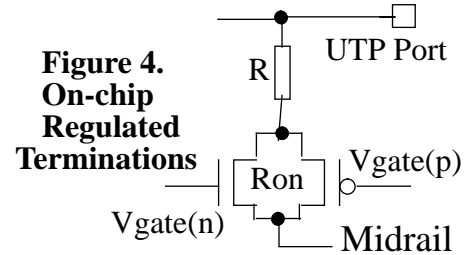
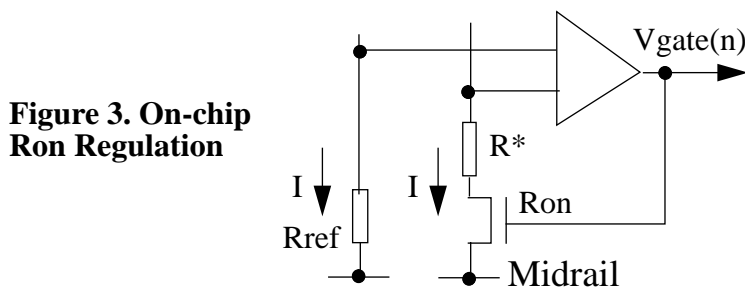
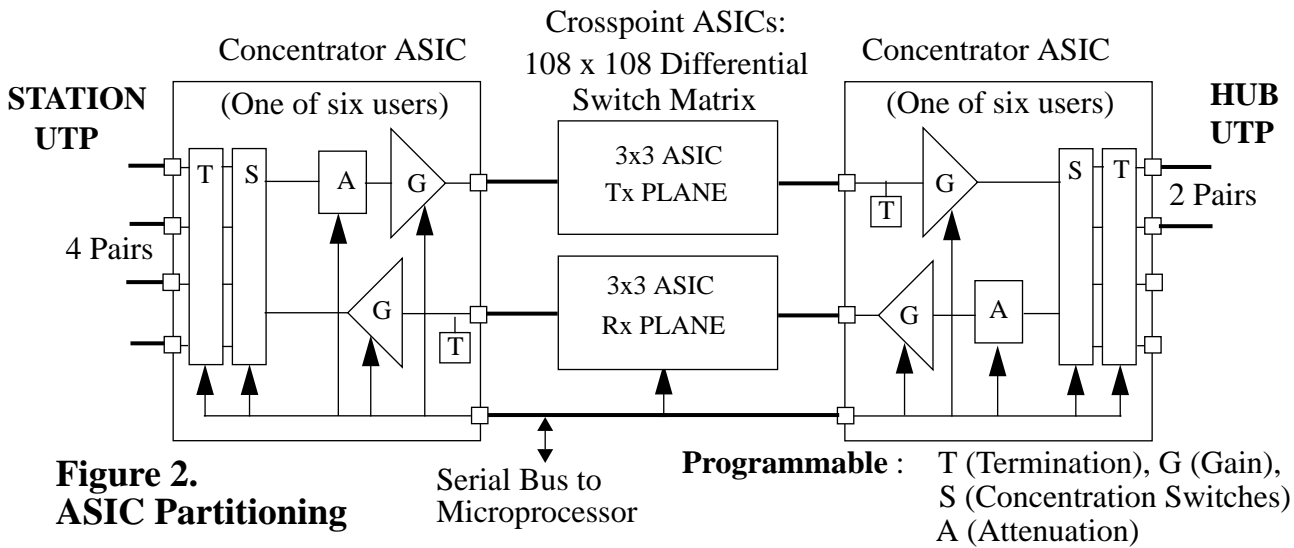
Half-Duplex operation was achieved using the circuit concept shown in figure 5. Both transmit and receive paths have signal detect circuits which monitor Tx/Rx signal activity. Once activity is detected the control logic turns on/off the appropriate switches to allow the signal to be correctly routed. When a signal is detected at 'A', the control logic turns ON the switches 'InA' and 'OutA' and the termination 'TermA'; while turning OFF switches 'InB' and 'OutB' and termination 'TermB'. A signal detected at 'B' causes the opposite switching. In addition to the signal being correctly routed, the control scheme ensures that the input is terminated and that the output has its termination removed - reducing power dissipation in the amplifiers.

Token-Ring operation, whilst using AC coupling to remove large CM voltage signals from the ASIC, is realized using the circuit concept shown in figure 6. Resistors R1, R2 mimic the load seen by a Station driving CM phantom current. Resistor R3 produces a small CM voltage offset (~100mV) which is applied to incoming data signals through on-chip terminations T. This offset voltage is passed through the crosspoint switch matrix and detected by a CM detection block which switches in a phantom current 'Ipc' to the Hub UTP cable. Thus the phantom current 'Ipc' is passed from Station to Hub without allowing large CM signals into the ASIC. The AC signals are referenced to the ASIC midrail supply by 100 ohm differential terminations.

In order to achieve 0dB insertion loss through-out the system, the Concentrator has a calibration system which includes an 8-bit A/D converter. This can be used to sense either internal DC calibration levels applied through the XPS, or the peak signal level from a user stored on an external capacitor. The attenuation and gain settings can then be adjusted to optimize the system for insertion loss, noise and crosstalk depending on the LAN standard used and magnitude of signal data. Table 2 summarizes the performance of the Concentrator ASIC.

**4. The Crosspoint ASIC:** This ASIC consists of a matrix of 36 x 36 differential 'T' switches which are controlled from a memory map via a serial data bus input. By implementing a 3x3 array of ASICs a 108x108 crosspoint switch matrix is generated, Figure 2.

These switches are NFET only in order to maximize bandwidth & are implemented in a checker board matrix of source & drains which minimizes capacitance & die area. The  $R_{on}$  resistance of crosspoint switches can vary by a large amount (typically +/- 50%) due to process variations. To overcome this variation, on-chip regulation shown in Figure 3 was used. The regulated  $R_{on}$  switches ensure uniform bandwidth, with signal path, due to the  $R_{on} \times C_{io}$  time constant associated with the switch; where  $C_{io}$  is the source/drain capacitance of the FET. To avoid  $R_{on}$  variation due to different metal track lengths (signal paths) within the crosspoint array, the switches are individually sized; switches with long input/output tracks are made larger (smaller  $R_{on}$ .) This sizing was achieved automatically, during the ASIC design phase, by generating a file of 36x36 signal path lengths & using this to control, via a layout macro, the size of the individual switches. Using these techniques the ASIC achieves a total switch resistance uniformity of less than +/- 2% across the die.



**5. Results:** Tables 2 and 3 summarize the ASIC performances. Figure 1 shows the Concentrator ASIC which is 10.6mm x 10.6mm in size. The six user segments can be clearly seen on the sides & top of the chip. Digital control to the users occupies the bottom segment. The 36x36 differential Crosspoint ASIC was realized in a die size of 6.5mm x 6.7mm. The ASICs operate successfully with all the stated LAN protocols and production of the product [1] has started.

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**References**

- [1] DynaTraX™ LAN cable management product, manufactured by NORDX/CDT, Inc., St.-Laurent, Quebec, Canada. (DynaTraX is a trademark of NORDX/CDT, Inc.)
- [2] C. Smythe, “Local-area network interoperability”, IEE Electronics & Communication Engineering Journal, August 1995, pp. 141-153
- [3] F. Barber et al., “A 64x17 Non-Blocking Crosspoint Switch”, ISSCC’88, Feb. 1988.

LAN	Vmax (Vp-p diff.)	Data Rate (Mbits/s)	Tx Mode
TP-PMD	2.1	100	Simplex
Ethernet	5.6	10	Simplex
IBM3270	4.3	2.358	Half-Duplex
IBM3XAS400	4.3	1.0	Half-Duplex
Token Ring	4.5*	4 or 16	Simplex

\* Note : Token Ring uses 4-7V DC Common Mode for normal Ring Insertion

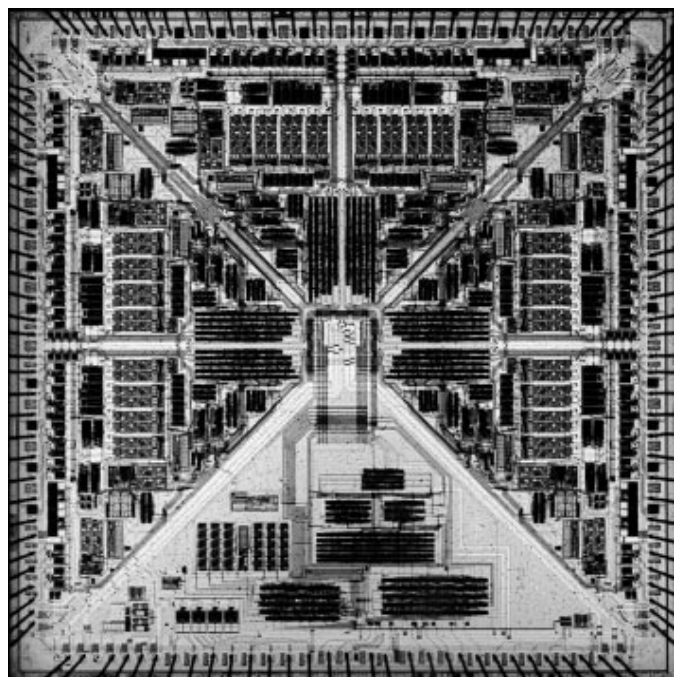
**Table 1 LAN Signalling Characteristics over 100m Unshielded Twisted Pair Cabling.**

Process:	SGS-T, 0.7um CMOS TLM
Die Size:	6.5mm x 6.7mm
Package:	160pin PQFP
Power:	< 100mW
Supply:	5.5V
Digital control:	2,800 gates, 1,300 memory elements
Analogue:	8000 devices
Switch Resistance:	260 Ohm differential
Switch Tolerance:	<5% (any path)
Switch I/O Capacitance:	19.5pF
Bandwidth:	140MHz, -3dB
Isolation:	-55dB @ 60MHz
Crosstalk:	-44dB @ 60MHz
I/P Voltage	< 2Vp-p for < 5% THD
Programming:	Read/Write, serial bus

**Table 3. 36x36 Differential Crosspoint Switch ASIC**

Process: (SGS-T)	1.2um BiCMOS DLM
Die Size:	10.6mm x 10.6mm
Package:	128pin PPQFP (Slug)
Power:	2 Watts maximum
Supply:	5.5V
UTP Cable drive:	30mA-p-p
Digital control:	4,500 gates, 500 memory elements
Analogue:	13,500 Devices
Op-Amps:	18 Current Feedback 110MHz BW, -3dB
Programmable:	
Terminations:	100 Ohms@<5% diff'tial
Attenuation:	0 to -9dB, 0.5dB steps
Transmit Gain:	0 to 9dB, 3dB steps
Receive Gain:	15dB to 30dB, 3dB steps
Programming:	Read/Write, serial bus

**Table 2 Concentrator ASIC**



**Figure 1. Concentrator Die Photo.**