

1 Gb/s clock recovery PLL in 0.5 μm CMOS

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Abstract

A clock recovery PLL is described for serial NRZ data transmission. The VCO works at only half the data rate, which means for a 1 Gb/s data rate the VCO runs at 500 MHz. A specially designed phase comparator uses both the rising and falling clock edges to compare clock and data. The VCO can typically be tuned from 350 MHz to 890 MHz and the PLL locks between 850 Mb/s and 1.3 Gb/s. The circuit consumes 140 mW (3.3 V) at 1 Gb/s including pad drivers.

1 Introduction

Digital signal processing is used more and more also in consumer applications. The main requirement there is low cost in mass production. Power consumption becomes an issue, as plastic packages are in use, and cooling measures like fans are to be avoided in many consumer products. In all portable applications, power is most critical.

Data transmission between different digital signal processing ICs influences significantly the power consumption and the system cost. For video signal transmission in 100 Hz TV sets typically 16 data lines in parallel are driven with 27 MHz rail to rail NRZ data signals. Sharp data transitions are in use to ensure reliable synchronous operation. A power saving alternative could be found in low swing high speed serial data transmission in the range of 500 Mb/s or more. However, this kind of high speed data transmission has to be asynchronous. To find an economic solution, we try to avoid separate transmission of the clock. Then, clock recovery from the NRZ data stream is required. In this paper we describe a PLL which was designed to process more than 1 Gb/s data in a 0.5 μm CMOS technology.

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2 Architecture

The phase comparator output signal properties are essential for the PLL operation. For very high operating frequencies analog signals depend on the data pattern and are highly non-linear. On the other hand, clock recovery schemes based on sampling techniques [1,2] result in identical digital control pulses. They are best suited to support highest possible data rates at a given technology. The key feature of our design is the phase-detector, which uses both the rising and falling clock edges. Therefore, the VCO runs at only half the data rate, which means that we can detect a 1 Gb/s serial data stream with a 500 MHz VCO. This relieves the timing constraints in the phase-detector logic and results in well correlated and data-independent control signals. Also, at the lower frequency the VCO-tuning range is larger and can compensate all technology parameter variations. With this architecture, we could achieve the highest data rates.

The block diagram of the circuit is shown in Fig. 1. No external components are required for the PLL. The loop filter capacitor was integrated on chip together with the VCO, the phase comparator and a charge pump. The data stream is sampled with the inverted and non-inverted clock, to provide two half speed retimed output data streams. A lock-in circuit is required and realized on chip, because our phase comparator is not frequency sensitive.

3 VCO

Both high oscillation frequency and a wide tuning range of the VCO are required. We choose a ring oscillator design with variable load capacitors (Fig. 2) based on [3]. This circuit can safely cope with all parameter variations. Fig. 5 shows the VCO tuning characteristic.

4 Phase Comparator

The phase comparator is an extension of the circuit from [1] to work with half the "normal" clock frequency (Fig. 3). The data stream is sampled at 4 identically spaced timepoints. The following logic circuitry generates the up and down control pulses for the VCO. They drive a current mirror charge pump [4] which assures that the charge delivered to the loop filter does not vary with the VCO control voltage.

The pulses are constant and do not depend on the data pattern. This generates a small jitter in the locked state. However, the magnitude is much smaller than the one introduced by data-dependent and non-linear analog pulses at high frequencies. Only rising signal edges are evaluated in order not to depend on duty cycle variations of the input signal.

For a small jitter absolutely identical sampling intervals are crucial. Therefore, a delay-line-loop (DLL) has been implemented to generate four 90° shifted clock phases $\text{clk1} \dots \text{clk4}$ from the VCO output signal. The stability of the system containing two coupled loops can be guaranteed because the DLL as a first order loop is inherently stable itself and different time constants for both loops are used.

5 Layout

In Fig. 4 the test chip is shown. A large area is used for the on chip loop filter capacitor (upper left). An equally big area is consumed by the ring oscillator with its load capacitors (lower left). Because the series resistance of those load capacitors is more critical than in the loop filter, a finer finger structure was chosen. All capacitors have been realized as MOS transistor gates. No special mask is required.

In the top right area the lock-in circuit and the DLL with its loop filter is located, whereas in the lower middle and to the right buffers and control logic can be seen.

6 Measurement Results

We verified locking of the PLL at data rates from 850 to 1300 Mb/s with a $(2^{31}-1)$ bit pseudo random sequence at the data input. Fig. 6 shows the regenerated clock compared with the data generator clock. The clock jitter is about 350 ps. Fig. 7 shows the locked PLL at 1 Gb/s and documents the correctly de-multiplexed output streams of the 111000 input sequence. The visible signal distortion is caused by the parasitic effects of the standard DIL 16 package used. Chip core area is 0.38 mm^2 , power consumption including output drivers is 140 mW at 1 Gb/s, $0.5 \mu\text{m}$ CMOS, 3.3 V supply. No external components are required, except one reference current, which is uncritical.

7 Conclusion

Complete on-chip clock recovery at 1 Gb/s is feasible with a standard $0.5\mu\text{m}$ CMOS technology. It enhances the power-saving high-speed asynchronous serial data transmission between integrated circuits.

Acknowledgments

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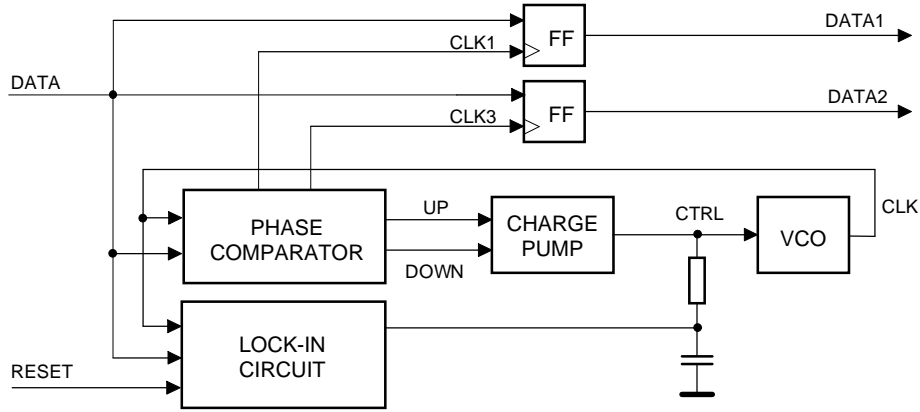


Fig. 1 Clock recovery block diagram

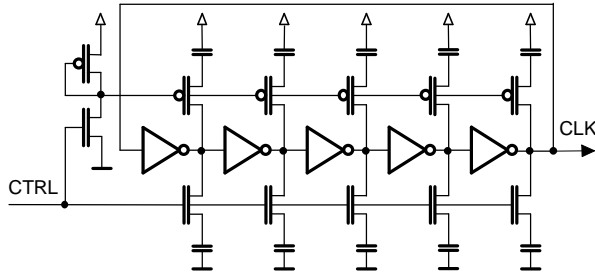


Fig. 2 VCO schematic

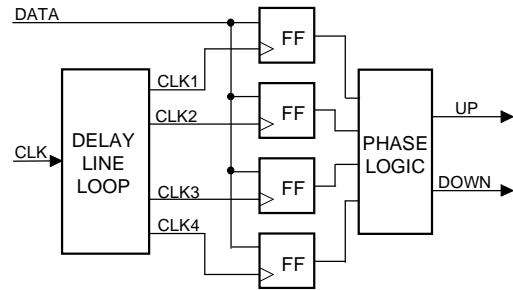


Fig. 3 Phase comparator

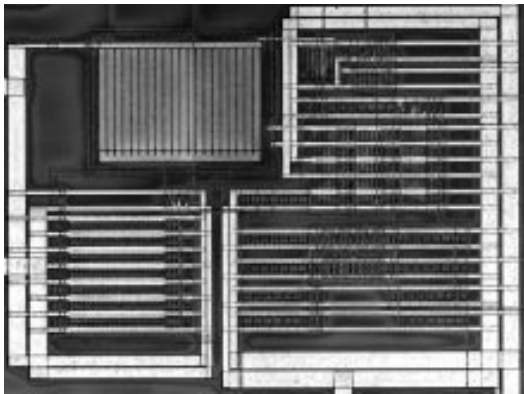


Fig. 4 Chip micrograph

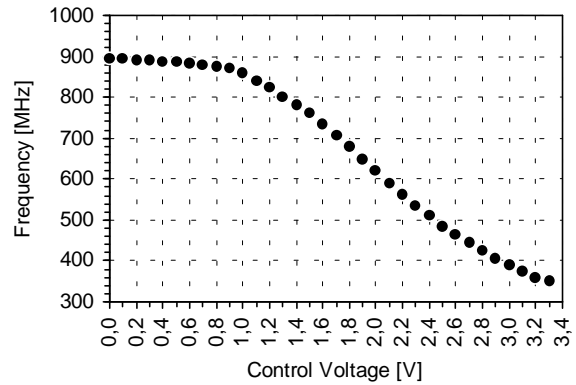


Fig. 5 VCO frequency vs. control voltage

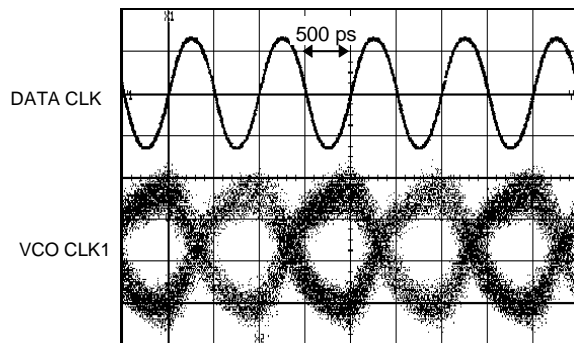


Fig. 6 VCO output clock eye pattern with a 2^{31} pseudo-random input sequence at 1 Gb/s

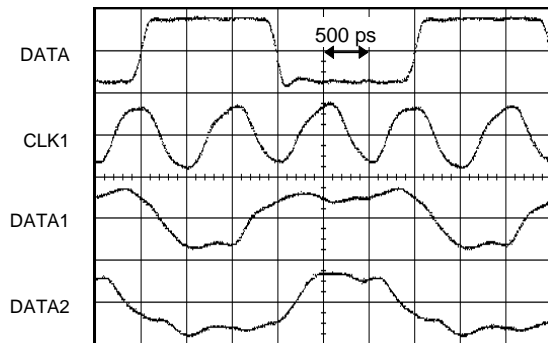


Fig. 7 111000 input pattern de-multiplexed in two data streams for off chip output at 1 Gb/s