A 3V 1 MHz dynamically biased 100ppm/K temperature-stabilized CMOS continuous-time elliptical low-pass filter

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A low voltage low power current-mode continuous-time elliptical low-pass filter is presented. This filter uses a current-integrator constructed of a multi-output linearized transconductance element driven by a balanced transimpedance amplifier. A 1 MHz third order elliptic low pass filter is designed with the proposed current-mode integrator. The filter measurements show capability of operation with down to a 3V supply voltage. The measured current consumption is 850 µA at room temperature and the dynamic range is 66 dB. The distortion of the filter is below 50 dBc with peak signal levels up to twice the quiescent current level. The filter uses a CMOS-current reference for temperature and process variation stabilization with a measured corner frequency temperature coefficient of -100ppm/K.

1 INTRODUCTION

Continuous-time integrated filters are realized typically with MOSFET-C or G_m-C techniques [1]. As supply voltages decrease it is increasingly difficult to produce the high control voltage needed to maintain the MOS-transistors in the triode region in MOSFET-C circuits. The G_m-C filters have relatively large distortion due to the open-loop operation of the integrators. Also many trans-conductance linearisation techniques used in the G_m-C filters have problems with operating at low supply voltages.

An alternative method to realize continuous time integrated filters is to use a current-mode integrator. Published current integrator based filters either have large distortion at large signal amplitudes [2] or the lossless integrator DC-gain is very sensitive to transistor mismatches [3]. In this paper we introduce an alternative current integrator which uses a linearized transconductance element inside a high gain current amplifier.

2. THE CURRENT-MODE G_m-C INTEGRATOR

2.1 Current vs. voltage signals in G_m-C integrators

Integrators can be constructed of transconductance amplifiers and capacitors with the G_m-C technique. However, there are two ways to realize these integrators using either voltage or current signals as shown in the lossy integrator implementations in Fig. 1.

The voltage-mode G_m-C integrator (Fig. 1a) can be transferred to a current-mode integrator (Fig. 1b) by changing the voltages to currents and changing the direction of the signals. With nonlinear

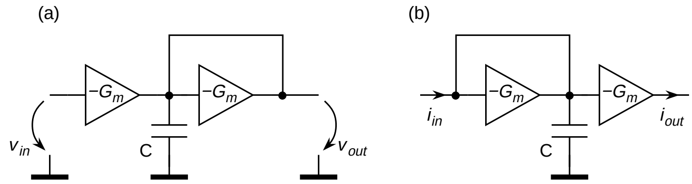

Fig. 1. Lossy G_m-C integrator using (a) voltage signals and (b) current signals.

transconductances the current-mode integrator has nonlinearity cancellation even at frequencies higher than the pole frequency unlike the voltage-mode integrator. Also the distortion at low frequencies is lower in the current-mode integrator due to the negative feedback like structure in Fig. 1b. A drawback in using the current-mode integrator is the need for multiple current outputs.

2.2 Multiple-output linearized transconductance element

For maximizing the voltage swing in the integrating node the linearization principle should use only transistors with their sources connected to the supply rails. The transconductance element should be easily multiplied and scaled in order to realize current-mode ladder filters. A linearization principle which meets these requirements is presented in Fig. 2. There are similar topologies using the push-pull class-AB configuration [4] or using transistors in the triode region [5]. This topology has also common-mode attenuation due to the partial common-mode feedforward effect [6].

The transconductance of the output MOS-transistors MP1A-MP2B is linearized by the dynamic biasing generated by the transistors MP3 and MP4 as follows

$$I_{D3} + I_{D4} = \frac{\beta_3 + \beta_4}{2} \left[v_d^2 + (V_{CM} - V_t)^2 \right]. \tag{1}$$

The equation shows that the quiescent bias current depends on the common-mode input voltage V_{CM} and that the bias current depends on the square of the differential input voltage v_d.

Respectively, the output current at one output branch is

$$i_{OA-} = 2 \beta v_d (V_{CM} - V_t), \tag{2}$$

if $\beta_{1A} = \beta_3 = \beta_4 = \beta$ and the NMOS current mirror mirroring ratio is 1/2. Ideally all nonlinearities are cancelled already in the single-ended output. The linearization accuracy is degraded by the transistor mismatches and phase errors due to the NMOS bias mirror but these errors are further reduced by the balanced structure.

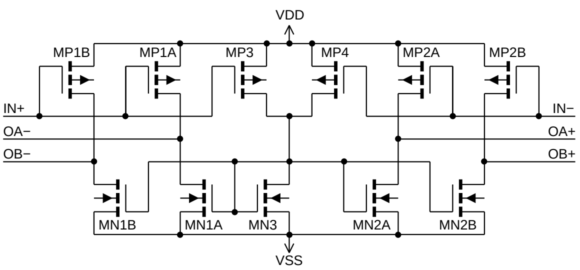

Fig. 2. The multiple-output dynamically biased transconductance element.

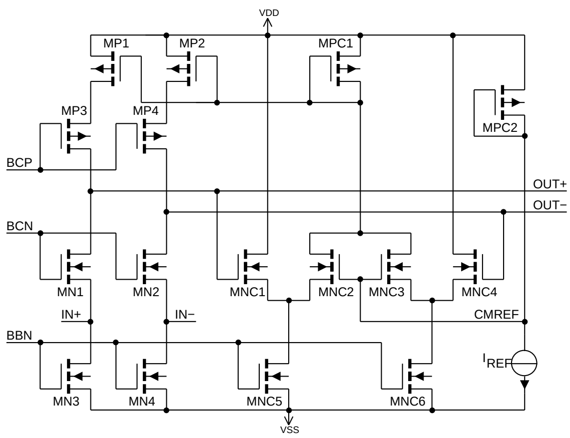

Fig. 3. Balanced transimpedance driver.

2.3 The transimpedance driver amplifier

Because the transconductance depends on the common-mode input voltage the driver amplifier has to set a well defined common-mode output voltage. The driver amplifier is presented in Fig. 3. It is a transimpedance amplifier with a common-mode feedback [4]. A high transimpedance is achieved with the cascode current source MP1-4 which is controlled by the common-mode sensing double differential pair MNC1-4. The common-mode reference voltage is set by a diode-connected transistor MPC2 and a reference current I_{REF} which is used to tune the transconductance of the integrator.

3 CURRENT-MODE ELLIPTICAL LADDER FILTER

The developed current integrator was applied to design a third order elliptical low pass filter. The passive prototype of the filter is presented in Fig. 5a and the current integrator ladder filter implementation of the prototype filter in Fig. 5b.

The time constants of the filter are adjusted by a transconductance stabilizing bias circuit in Fig. 4 using one off-chip resistor R_{EXT} [7]. This biasing technique reduces the temperature dependency of the filter time constants down to approx. -70 ppm/K in simulations and -100 ppm/K in measurements. Although the CMOS current reference can reduce temperature and process variation dependencies of the filter but cannot reduce the dependency on the capacitance variation. This variation can be tuned in testing phase with the external resistor R_{EXT}. The absolute accuracy, however, is without trimming more than enough for anti-alias and smoothing applications. The measured frequency responses agree with with the simulations (Fig. 6)

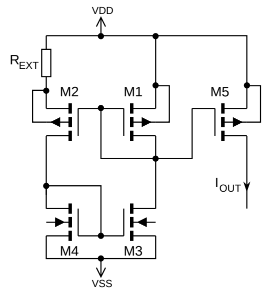

Fig. 4. The filter bias current generation principle

The quiescent current of the output transistors of the integrators are nominally 10 µA. The filter operates with a down to 3V single supply and the current consumption of the whole filter with interfaces is 850 µA in room temperature (only the filter 230 µA/pole). The measured total harmonic distortion in Fig. 8 is below -40 dB up to the signal peak level of 60 µA which is 50% more than the theoretical maximum of the linearisation principle. The measured dynamic range of the filter is 65.5 dB.

The filter is fabricated with a 1.2 µm CMOS-process. The microphotograph of the filter is presented in Fig. 9 and the area of the whole chip is 2.2 mm^2 and the actual filter area is 0.15 mm^2/pole.

4 CONCLUSIONS

The proposed current integrator based filter promises competitive speed, dynamic range and current consumption to G_m-C filters with low distortion. It also operates at lower supply voltages than most G_m-C filters. The designed filter can be realized also as a transistor-only filter with a digital CMOS-process if transmission zeroes are not needed. The frequency range of the presented filter can also be realized by utilizing the BiCMOS-process.

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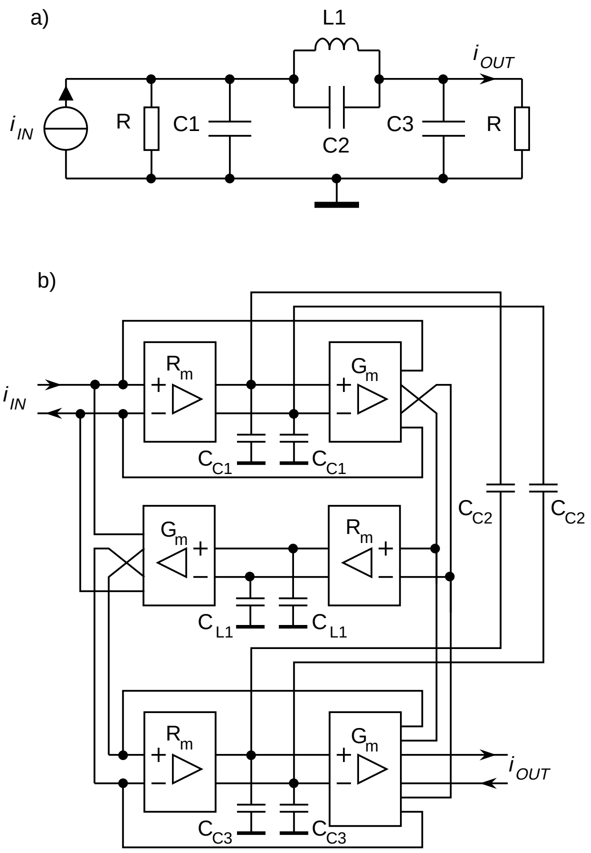

Fig. 5. The current integrator based elliptic ladder filter realization.

Table 1 Filter performance.

Technology	1.2µm CMOS
Chip area (all) (per pole)	2.2 mm^2 0.15 mm^2
Power supply	3.3V ±10%
Current consumption (the whole chip) (per pole)	0.85mA@+27°C 0.68mA@-20°C 1.06mA@+80°C 230µA@+27°C
THD (f=100kHz)	-47dB@120µApp -52dB@40µApp
IM3 (f1=250kHz, f2=400kHz)	-54dB@120µApp -65dB@40µApp
Dynamic range	65.5dB

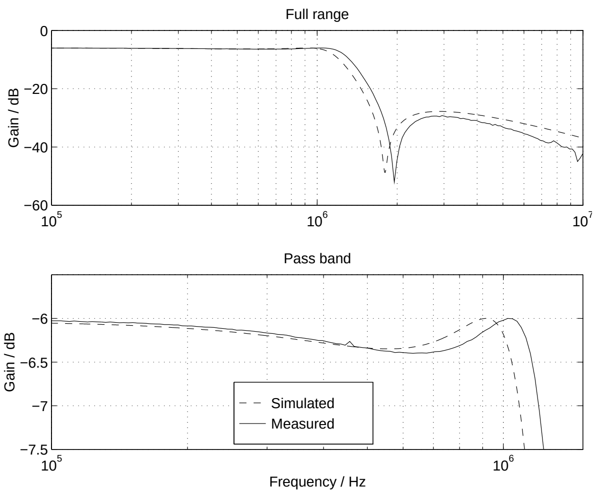

Fig. 6. The measured frequency response of the filter.

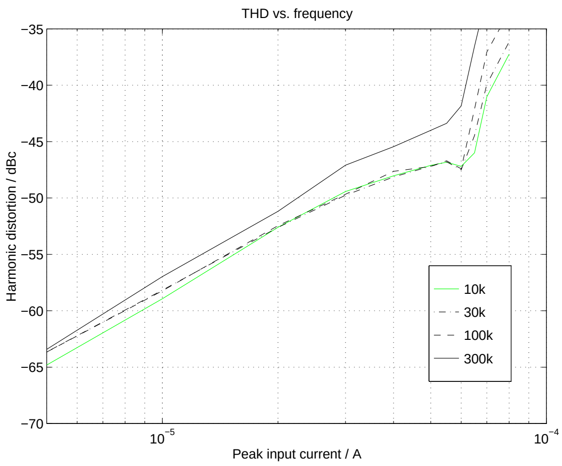

Fig. 7. The measured THD vs. input signal level with 10k, 30k, 100k and 300kHz signals.

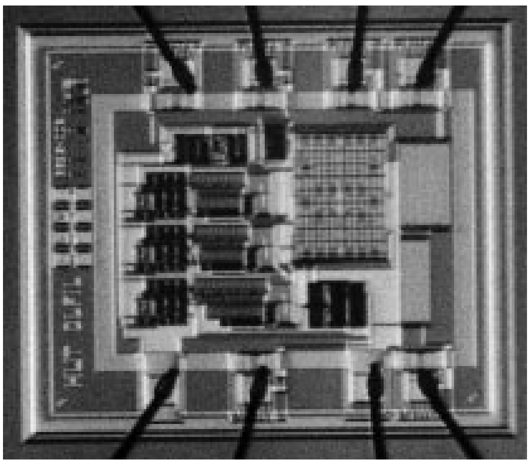

Fig. 8. The microphotograph of the chip.