Thermally Constrained Placement of Analog and Smart Power Integrated Circuits

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Abstract: This paper presents an algorithm for the performance driven placement of temperature sensitive analog integrated circuits. A simulated annealing algorithm is used to optimize an initialy random placement. During each iteration of the optimization algorithm, the temperature distribution caused by power dissipating devices is calculated using an analytical multi-layer thermal model. The influence of local temperature differences on the performance of the circuit is then computed using sensitivity information and specification violations are penalized in the placer's cost function. In this way, it is guaranteed that the thermally-induced performance degradation, such as offset, stays within the specifications of the designer. An industrial circuit is used to verify the algorithm.

1 Introduction

A current trend in IC technology is the integration of power devices together with complex digital and high-performance analog circuits on the same chip. Examples can be found in such diverse applications as smart power IC's, telecommunication circuits and high-speed memories and microprocessors. The increasing power densities on these chips are reaching levels where parasitic thermal effects limit performance. When power is dissipated within a device on the surface of an integrated circuit die, the generated heat must flow away through the silicon material. This heat conduction gives rise to a temperature distribution across the chip. Since device parameters are affected by local temperature fluctuations, the performance of the whole circuit is influenced. Thermal effects cause input offset voltage in differential amplifiers [1], reference voltage shifts in regulators [2] and loss of dc gain in operational amplifiers [1]. To control this thermally-induced performance degradation, it has become essential to take thermal effects into account during layout design.
In [3], a performance-driven placement tool, capable of controlling performance degradation due to interconnect parasitics and device mismatches was presented. In this paper, we extend this methodology to also handle performance degradation induced by thermal effects. In section 2 we give an overview of the placement algorithm and the modifications necessary to handle thermal effects. In section 3 we explain how thermally-induced performance degradation can be computed using an efficient and accurate thermal modeling technique. An example of a temperature sensitive analog circuit, placed with the tool is presented in section 4.

2 Placement Methodology

The basic components of the placement algorithm are shown in Fig. 1. The first step in the execution of the program consist of a number of numerical simulations to determine the necessary information for the computation of thermally induced performance degradation. The power

dissipation in each device is measured as well as the sensitivities of performance characteristics to local temperature fluctuations. During each simulation, the temperature of one or more transistors is modified and the influence on the performance of the circuit is determined.
After circuit analysis, device generators are called in interface mode to generate a list of possible geometrical variants for each device. For each variant, the geometrical and thermal information relevant for the execution of the placement algorithm is generated : the bounding box, terminal protection frames and a thermal matrix . The thermal matrix describes the temperature profile caused by the power dissipation in the variant.
A simulated annealing algorithm is then used to optimize an initial random placement. During each iteration of the optimization algorithm, the temperature distribution of the placement is calculated by superposition of the individual profiles of each power dissipating device. The local temperature of each device in the placement together with the predetermined temperature sensitivity is then used to determine the thermally induced performance degradation. If a performance specification is violated, a penalty proportional to the amount of violation is inserted into the cost function. In this way, all specification violations are driven to zero in the final result and it is guaranteed by the tool that all thermal effects ar within the allowed margins. For this algorithm to work in acceptable CPU time, a fast and reasonably accurate calculation of the local temperature distribution for intermediate placement solution is needed. This will be discussed next.

3 Thermal Modeling of Integrated Circuits

Fig. 2 shows a schematic representation of a multilayer electrothermal integrated circuit structure with a central square surface heat source on top. The different layers model the differents parts of the integrated circuit structure, such as the silicon chip, the die-bonding layer and the package. Within every layer, the material is assumed to be linear, isotropic and homogeneous. To obtain the static temperature distribution for this problem, the following heat-flow equation has to be solved :

$$\nabla^2 T(x, y, z) = 0 \quad (1)$$

with adiabatic side walls, an isotherm bottom surface and natural convection at the top as boundary conditions. Power is generated uniformly in the surface source with power density Q_0''. With these assumptions, the temperature distribution on the top surface of the N-layer structure can be written as a double Fourier series [4]:

$$T(x, y) = \frac{4Q_0''}{k_N} \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \tau_N(n, m) \cdot \frac{\sin \frac{n\pi w}{L_x}}{(1 + \delta_{n0})n\pi} \cdot \frac{\sin \frac{m\pi h}{L_y}}{(1 + \delta_{m0})m\pi} \cdot \cos \frac{n\pi x}{L_x} \cdot \cos \frac{m\pi y}{L_y} \quad (2)$$

where L_x,L_y and w,h refer to the dimensions of the chip and the source respectively (see Fig. 2). The Fourier coefficients $\tau_N(n, m)$ depend upon the thermal conductivities k_i and thicknesses L_i of the layers in the multilayer structure and can be computed with the following recursive relation :

$$\tau_1(n, m) = \tanh(\gamma(n, m)L_1) \quad (3)$$

$$\tau_N(n, m) = \frac{k_{N-1} \tanh(\gamma(n, m)L_N) + k_N \tau_{N-1} \gamma(n, m)}{k_{N-1} + k_N \tau_{N-1} \tanh(\gamma(n, m)L_N)} \quad (4)$$

$$\gamma(n, m) = \sqrt{\left(\frac{n\pi}{L_x}\right)^2 + \left(\frac{m\pi}{L_y}\right)^2} \quad (5)$$

We use the two-dimensional Fourier series (2) as the basis for an efficient thermal computation scheme :

1. We start with computing a thermal model for a unit source by evaluating series (2) on a grid of points $(x_i, y_i), i = 0 \cdots n-1$. The result is stored in a $n \times n$ matrix T_u. This is a computationally expensive step since the series (2) has to be evaluated to a high order. It must be noted however, that this computation has to be done only once for a given layered structure. The resulting T_u matrix can be reused for other placement problems on the same electrothermal structure.

2. During the device initialization phase, the active surface of a variant, which can have any rectilinear shape, is discretized into a collection of unit sources. The contribution of each unit source is given by T_u, shifted in position and multiplied with the power density of the device. By adding up the contributions of the unit sources, the thermal profile of the variant can be evaluated and stored in its thermal matrix. This computation has to be done once for each variant. The resulting matrix can be reused throughout the placement.

3. During the annealing loop, the temperature distribution of an intermediate placement can be calculated by superposition of the individual devices' thermal profiles. This can be done very fast since the thermal profiles were precomputed and stored in the thermal matrices of the variants. This gives the local temperature of every device for the given placement, from which the thermally-induced performance degradation is calculated.

4 Experimental results

We used this algorithm to generate the placement for the class AB operational amplifier shown in Fig. 4. The power consumption of the circuit is $140mW$, of which most is dissipated in the output stage $M14, M15, M16, M17$. An offset voltage of less than 5 mV is specified. The placement of the circuit is shown in Fig. 5 and the resulting thermal profile in Fig. 6. Table 1 gives the sensitivities, the temperatures and the resulting offset voltage degradation for the most sensitive transistor pairs in the circuits. It can be seen from the layout that the sensitive transistor pairs have been placed symmetrically with respect to the output transistors.

5 Conclusions and Future Work

We have presented a placement tool, capable of controlling thermally induced performance degradation. Using an accurate and efficient thermal modeling technique, temperature distributions and resulting performance degradations can be computed during placement optimization. The effectiveness of the approach was demonstrated with an industrial circuit.

Acknowledgements

This research is supported by ESA-ESTEC and by the CEC ESPRIT project ADMIRE.

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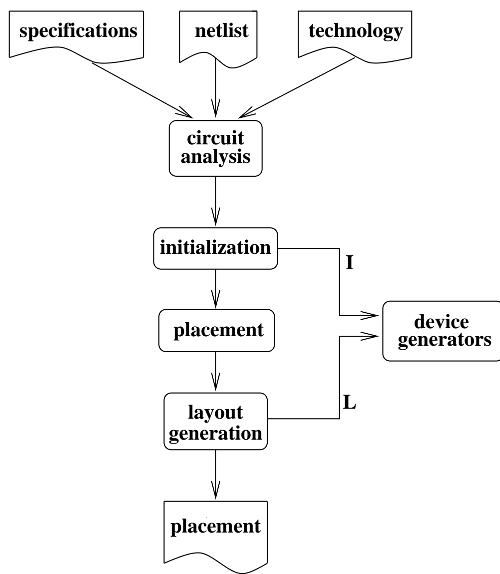

Figure 1. Overview of the placement program

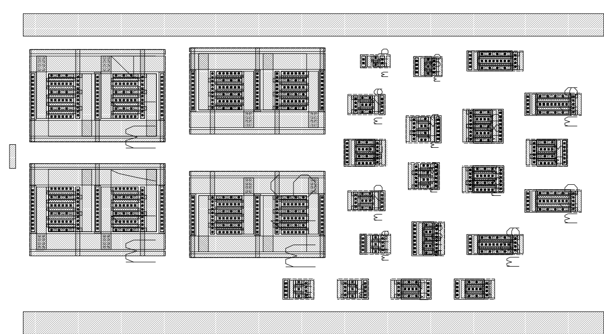

Figure 4. Placement of the class A/B operational amplifier

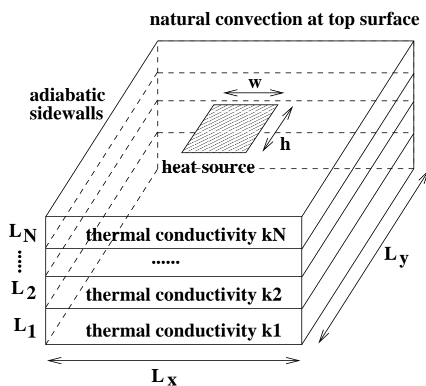

Figure 2. Multi-layer thermal model for an integrated circuit device

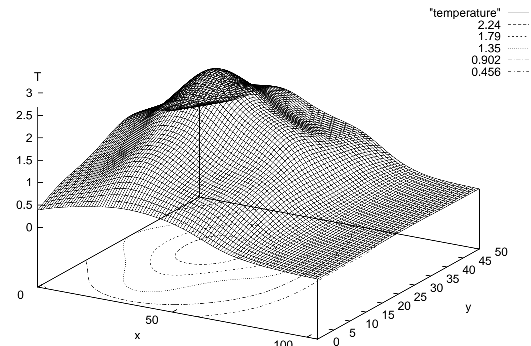

Figure 5. Temperature distribution of the class A/B operational amplifier placement

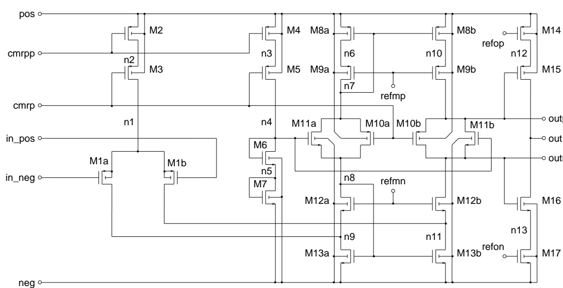

Figure 3. Schematic of the class A/B operational amplifier

opamp offset voltage			
Trans. Pair	Sens.	Temp. Diff.	Degr.
	$\frac{mV}{\text{deg}}$	deg	mV
$M1a - M1b$	1.6	0.153	0.245
$M8a - M8b$	3.7	0.084	0.319
$M13a - M13b$	6.0	0.074	0.448
total			1.012

Figure 6. Thermally induced performance degradation for the offset voltage of the opamp.