

# CMOS Current Reference without Resistance

H. Oguey and D. Aebischer

Swiss Center for Micro-Electronics and Microtechnology (CSEM)  
 Maladière 71, CH-2007 Neuchâtel, Switzerland  
 tel. +41 38 205 111  
 fax. +41 38 205 770  
 Email: daniel.aebischer@csemne.ch

A micropower current reference can be built with CMOS transistors only. It shows low sensitivity with respect to technology, supply voltage and temperature, and it works on very low supply voltages. The circuit is very simple and occupies a small surface area.

## 1. Known circuit.

A current reference is a basic building block in analog circuits. It is needed for oscillators, amplifiers, PLL's, etc. A good reference should be based on intrinsic physical properties, independent of technology. This is possible for voltage references, based on CMOS-compatible bipolar transistors. But current references are generally derived from voltage references by means of an additional voltage to current converter [1]. A well known circuit which uses MOSFETs only and one resistor [2] is shown on Fig. 1a.

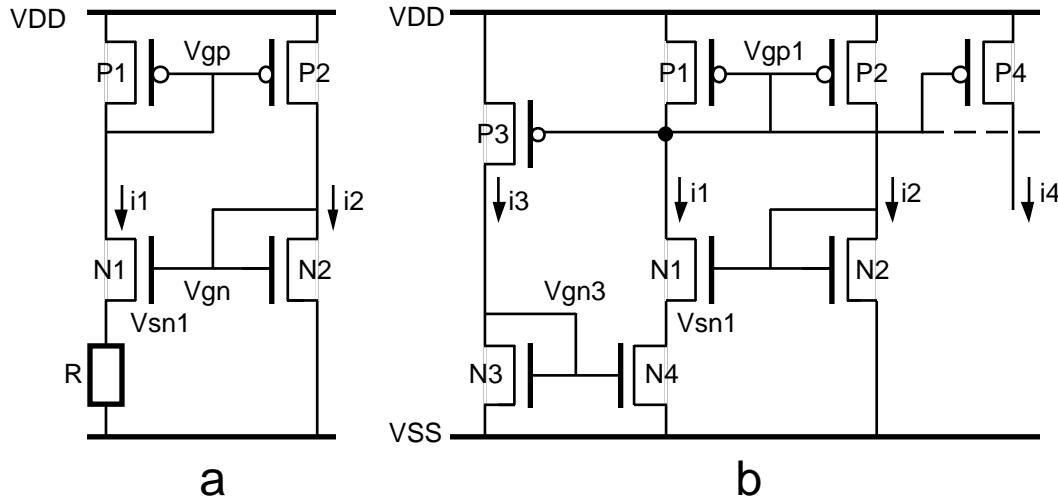


Figure 1. CMOS current references. a) Known circuit with resistance.  
 b) New circuit with CMOS transistors only.

P-channel MOSFETs P1 and P2 act as a current mirror. The source voltage of N1 is given by

$$V_{Sn1} = U_T \ln \left( \frac{S_{N1} S_{P2}}{S_{N2} S_{P1}} \right) \quad (1)$$

where  $U_T = kT/q$  and  $S_{N1}$ ,  $S_{N2}$ ,  $S_{P1}$ ,  $S_{P2}$  are W/L ratios of the respective MOSFETs.

Notice that  $V_{Sn1}$  does not depend upon the current level, as long as N1 and N2 are in weak inversion. Its value is in the range of 40 to 80 mV at room temperature. The current  $i_1$  is defined by R, and can be reproduced by further current mirrors associated with the N-channel or the P-channel MOSFETs.

The presence of a resistance is a drawback for some applications. If a low current is required, a high value resistance is needed. If it is made with drain diffusions or highly doped polysilicon, it takes a large surface area. The resistivity is not guaranteed by some foundries and can vary with the technology. The temperature coefficient is not well defined and does not compensate for the temperature dependence of  $V_{Sn1}$ .

## 2. New current reference circuit.

The new current reference generator proposed here [3] (Fig. 1b) is based upon the same circuit as in Fig. 1a, except that the resistance is replaced by a n-MOSFET N4 working below saturation, and contains 2 additional MOSFETs in order to provide a gate voltage for N4. P3 delivers a current  $i_3$  proportional to  $i_1$ . This current passes through N3, who has its gate connected to its drain and to the gate of N4.

It is assumed that N3 is saturated, while N4 has a low drain voltage equal to  $V_{Sn1}$ . The following relations apply if N3 and N4 are in strong inversion:

$$i_3 = \frac{1}{2} \beta_{n3} (V_{Gn3} - V_{Tn})^2 \quad (2)$$

$$i_1 = n \beta_{n4} V_{Sn1} (V_{Gn3} - V_{Tn} - \frac{n}{2} V_{Sn1}) \quad (3)$$

Starting with a given value of  $i_1$ , current mirror P1-P3 defines  $i_3$ , and elimination of  $V_{Gn3} - V_{Tn}$  gives a new value  $i_1'$ .

$$i_1' = n \beta_{n4} V_{Sn1} \left[ \sqrt{\frac{2i_1 S_{P3}}{\beta_{n3} S_{P1}}} - \frac{n}{2} V_{Sn1} \right] \quad (4)$$

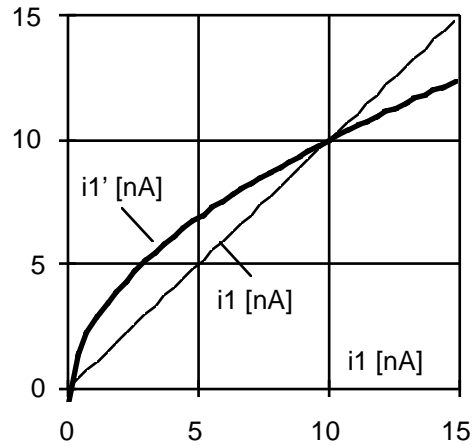


Fig. 2 shows that two crossing points exist between  $i_1$  and  $i_1'$ . The stable solution corresponds to the upper one.

Figure 2. Characteristics  $i_1$  and  $i_1'$  show crossing points given by (4)

A closed form solution, taking (1) and (4) into account, gives the current  $i_1$ :

$$i_1 = n^2 \beta_{n4} U_T^2 K_{\text{eff}} \quad (5)$$

$$\text{with } K_{\text{eff}} = \left[ K_2 - 0.5 + \sqrt{K_2(K_2 - 1)} \right] \ln^2(K_1) \quad (6)$$

$$K_1 = \frac{S_{N1} S_{P2}}{S_{N2} S_{P1}} \quad K_2 = \frac{S_{N4} S_{P3}}{S_{N3} S_{P1}} \quad (7)$$

The current  $i_1$  is proportional to the effective gain factor  $n^2\beta_{n4}$ , to the square of the thermodynamic voltage  $U_T$  and to a factor  $K_{\text{eff}}$ , which is a function of the geometrical ratios, and is therefore very stable. This current is independent of the threshold voltages. The effective gain factor  $n^2\beta_{n4}$  is very reproducible in a standard CMOS technology, if N4 is drawn with non-minimum dimensions.

### 3. Temperature dependence.

It is known that the gain factor varies with temperature in the same way as the mobility:

$$\beta_{n4} = \beta_{n40} \left( \frac{T_0}{T} \right)^m = \beta_{n40} \left( \frac{U_{T0}}{U_T} \right)^m \quad (8)$$

where  $\beta_{n40}$ ,  $T_0$  and  $U_{T0}$  are defined at room temperature, and  $m$  is close to 2. The current  $i_1$  becomes

$$i_1 = n^2\beta_{n40}U_{T0}^2K_{\text{eff}} \left( \frac{T}{T_0} \right)^{2-m} \quad (9)$$

Due to the small value of the exponent  $2-m$ , the current  $i_1$  is fairly stable with temperature.

### 4. Design considerations

It is important to verify that N1 and N2 work in weak inversion, whereas N3 and N4 work in strong inversion. A continuous model of the MOSFET [4] helps to find the limits of these domains. By comparing the simple expressions with the accurate ones, the limits of validity, for a given accuracy, can be deduced.

Example: conditions for a relative current error  $< 5\%$ :

1. Weak inversion, saturation:  $\frac{i}{n^2\beta} < 6 \cdot 10^{-6} \text{ V}^2$
2. Strong inversion, saturation:  $\frac{i}{n^2\beta} > 2 \cdot 10^{-2} \text{ V}^2$
3. Strong inversion, below saturation:  $\frac{i}{n\beta(V_D - V_S)} > 0.18 \text{ V}$

In order to obtain the most satisfactory results, it is advisable to group the components:

Group MNA: N1 and N2 (weak inversion)

Group MNB: N3, N4 and further current sinks (strong inversion).

Group MP: P1, P2, P3 and further current sources (strong inversion).

In each group, the transistors have the same gate voltage and are decomposed into identical unit transistors of exactly the same geometry and orientation. Table 1 is a design example.

Group	MNA	MNA	MNB	MNB	MP	MP
MOSFET	N1	N2	N3	N4	P1, P2	P3
W ( $\mu\text{m}$ )	6*100	100	4	4	4	4*4
L ( $\mu\text{m}$ )	4	4	710	710	300	300
$i_1 / n^2\beta$ ( $\text{V}^2$ )	1 $10^{-6}$	6 $10^{-6}$	0.1		0.015	0.015
$i_1 / n\beta V_D$ (V)				0.32		

Table 1. Example of dimensions for a current reference of 10nA in a 2 $\mu\text{m}$  technology.

## 5. Experimental data

This circuit has been integrated with non-optimum dimensions in a  $2\mu\text{m}$  CMOS technology. Fig. 3 presents the theoretical and experimental current as a function of temperature. A reasonable concordance is found. The slopes of these curves corresponds to  $m=1.5$ . A drop of the current above  $60^\circ\text{C}$  is attributed to a pad protection, and is not likely to exist in the circuit itself.

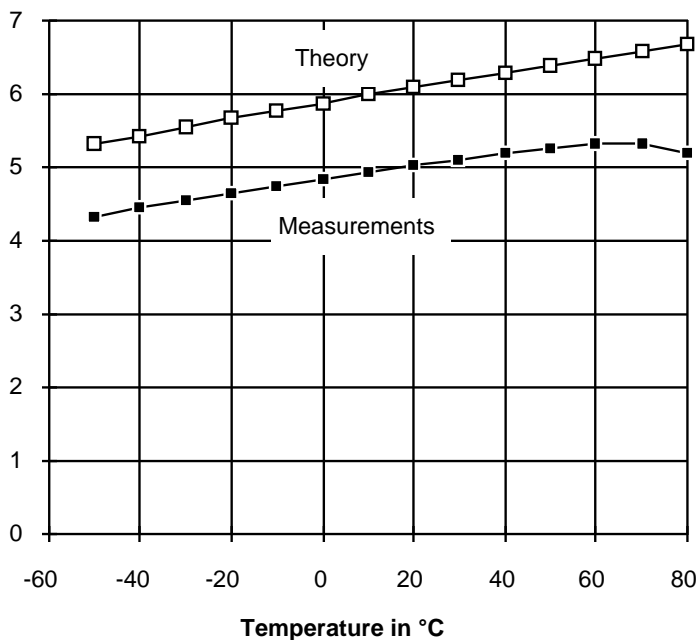


Figure 3. Theoretical and measured current in function of temperature.

Theory corresponds to  $m=1.5$

A fairly large spread in current values from circuit to circuit was observed. With a careful layout design according to the above considerations, a tolerance of about  $\pm 30\%$  should be feasible.

This autonomous circuit will find applications where a very small bias current has to be generated by simple means.

## References

- [1] E. Vittoz, "The design of high performance analog circuits on digital CMOS chips", *IEEE Journal of Solid State Circuits*, Vol. SC-20, No 3, pp. 657-665, June 1985.
- [2] E. Vittoz and J. Fellrath, "CMOS Analog Circuits Based on Weak Inversion Operation", *IEEE Journal of Solid State Circuits*, Vol. SC-12, No 3, pp. 224-231, June 1977.
- [3] French Patent Application F 95 03352.
- [4] E. Vittoz, "Low power design: ways to approach the limits", Proc ISSCC, February 16, 1994.