

# A DSP-Based Digital IF AM/FM Car-Radio Receiver

F. Adduci, M. Annovazzi, G. Boarin, A. Colaci, V. Colonna, G. Gandolfi, M. Sala, F. Salidu, F. Stefani  
 STMicroelectronics - Via Tolomeo, 1 - 20010 Cornaredo (MI) - Italy

M. Frey, P. Kirchlechner, C. Kutschenreiter

STMicroelectronics – Werner-von-Siemens-Ring, 3-5 – 85630 Grasbrunn - Germany

A. Baschirotto

University of Lecce - Department of Innovation Engineering - Via per Monteroni - 73100 Lecce, Italy

## Abstract

This paper describes the design and the implementation of a DSP-based digital IF (Intermediate Frequency) radio receiver in a low-power 0.18 $\mu$ m CMOS technology. Thanks to an advanced System-on-Chip mixed analog and digital solution, the proposed device performs the demodulation of both AM and FM stereo signals, digitized at the IF by means of a high dynamic range  $\Sigma\Delta$ -bandpass analog to digital converter. The chosen architecture combines hardware and software functions, yielding true blind equalization of the FM channel; this results in an outstanding rejection of the adjacent channels and of any other interfering signal, even under severe multipath conditions. The described chip occupies as small as 15.21mm<sup>2</sup> and it is shipped in a compact 64-pin package, reducing application costs while ensuring state-of-the-art performance.

## I. Introduction

Nowadays, in the AM/FM radio receiver scenario the general trend aims at the software radio, a fully digital solution encompassing RF digitization and signal processing in a DSP. This target appears very challenging for state-of-the-art technologies; therefore, intermediate solutions, as in Fig. 1 and [1-3], are being developed exploiting the advantages of scaled-down technologies. The digital-IF reception is competitive with respect to traditional analog solutions as it implements a flexible and superior digital processing in a reduced die area, and at lower power consumption.

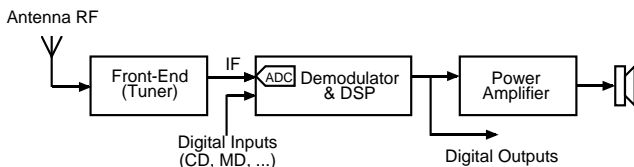


Fig. 1 - Car-radio receiver with IF digitalization

The block diagram of the proposed high-performance radio receiver is shown in Fig. 2. The relevant features of this device are listed below:

- the IF-ADC converter, the quartz-based oscillator and the AGC-keying DAC are the only analog blocks.
- the 24-bit DSP core allows enough computing capability for implementing complex processing algorithms as true blind channel equalization, spike detection and correction, noise blanking and audio functions.
- the DSP peripherals operate as software-controlled hardware accelerators, used to implement basic radio-functions as AM/FM detection, stereo channel separation and Radio Data System (RDS) demodulation and decoding.

- multiple communication interfaces are available: I2C or SPI for memory load and run-time control, SAI for audio data transmission, ASRC for internal sample rate conversion and HS3I for high sample rate data transfer.
- the device either operates as a stand-alone AM/FM stereo radio receiver or it is used in an array system for high-end dual tuner diversity applications. In the latter case, two devices are connected together working in a master-slave configuration, where the master chip is responsible for the two IF-channel equalization and mixing, and the slave chip acts as a co-processor.

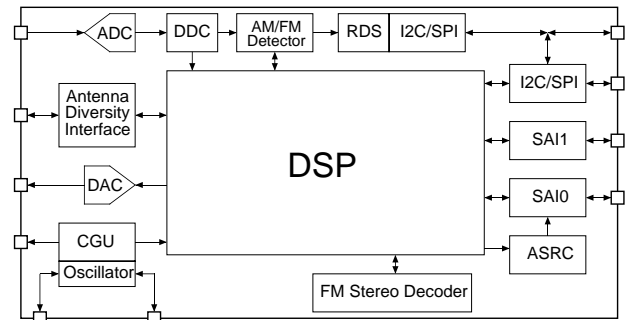


Fig. 2 - Overall single-chip radio architecture

## II. Functional Description

The 10.7MHz IF-signal is digitized independently from the type of modulation. The digitized signal is down-converted to zero-IF by means of a Digital Down Converter (DDC) as shown in Fig. 3.

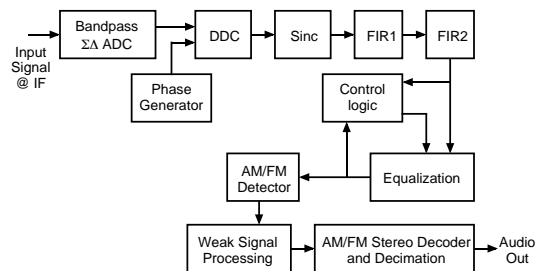


Fig. 3 - Simplified demodulator block diagram

The DDC transforms the wide-band real IF input into a quadrature complex base-band signal, selecting the narrow-band frequency of interest. High linearity and performance in the down conversion are achieved thanks to a COordinate Rotation DIGital Computer (CORDIC) [4] resulting also in smaller hardware complexity with respect to the conventional digital mixer architecture. Prior to demodulation, proper channel filtering is required, in order to reduce the signal bandwidth and the sample rate [5]; this is accomplished by cascading a 5<sup>th</sup>-order Sinc filter, [6], a finite impulse response filter (FIR1) compensating the Sinc

drop, and a second low-ripple FIR (FIR2), used to select the signal bandwidth of interest (about 300kHz). This solution simplifies the design of the analog front-end, since only one external ceramic filter is required; this filter protects the tuner IF-amplifier and the IF-ADC from strong interfering signals, without constraints on channel selectivity. After the channel selection by means of the DDC, a high sampling rate signal processing is required.

In the case of FM, the incoming signal is properly equalized for improving the reception quality. The chosen algorithm is a special kind of channel equalizer, known as *blind* equalizer, since it does not require the transmission of any training sequence. Actually, both the broadcasted signal and the channel impulse response are unknown a-priori; therefore the blind equalizer recovers the signal on the basis of statistical properties of the input sequence. Among the large class of blind equalization algorithms, the Constant Modulus Algorithm (CMA) [7] has been used since it is well suited for FM signals, exploiting the constant modulus property. The CMA adapts the coefficients of a SW-implemented FIR in order to compensate the transmission channel transfer function, coping with additive noise, multipath fading and adjacent channel interference. On the other hand, a CMA is not sufficient in an FM radio broadcasting scenario; in fact, multiple FM signals (the desired channel and its neighbors) with the constant modulus property are present at the equalizer input, and the CMA converges to the highest energy signal. In our system, an innovative controlling algorithm has been devised to detect and prevent such a condition.

The equalizer filter is implemented as a finite-length FIR; therefore, the channel transfer function cannot be completely compensated; as a consequence, the equalizer cannot remove instantaneous spike noise affecting the composite signal recovered by the AM/FM detector. Spikes are mainly originated by the electromagnetic fields due to fast current variations and to the high current discharges in the ignition phase of the car engine. A dedicated algorithm for spike detection and suppression has been developed. In the FM baseband processing, the stereo-decoder is hardware implemented, since on-field tuning is not required.

AM signals cannot be equalized according to the constant module property, thus only additional channel filtering after the DDC is performed before demodulating the complex signal in the AM/FM detector.

The spike-detection and noise blanking for both AM and FM are software implemented yielding customizability depending on field conditions. Finally, for FM signals, RDS filter, demodulator and decoder modules are hardware implemented and the RDS output data is available through either I2C or SPI interface; instead, in case of AM, superior ISB and CQUAM processing are available on the DSP.

The master clock is chosen to be 74.1MHz since its harmonics fall outside the worldwide FM bandwidth, and it equals two times the ADC sampling frequency (see III.b); according to this, there is no need for a phase-locked loop (PLL) because all the required clocks are obtained by dividing the master clock. The companion tuner-chip receives its reference clock through a differential interface allowing the overall system to save one additional crystal for the tuner.

A standard I2C/SPI interface is available for the communication with an external microprocessor or memory.

### III. Analog Blocks

#### III.a Clock generation unit (CGU) and oscillator

This module generates all the clocks and synchronization signals for the device and the reference VCO clock for the tuner. The quartz-driven 74.1MHz oscillator works at the 3<sup>rd</sup> overtone. In order to guarantee maximum performance of the IF-ADC, the oscillator has been designed with less than 15ps rms frequency-jitter; in addition, high frequency stability over temperature is obtained exploiting a constant-gm circuit. In slave-mode the oscillator behaves as a buffer, and an external clock drives the chip.

The CGU is responsible of both controlling the oscillator and generating clocks for DSP peripherals. It implements a self-trimming algorithm assessing the bias currents used in the oscillator, allowing the master clock frequency to be unaffected by process parameter variations; in addition, the DSP itself is allowed to control the fine adjustment of the bias currents with 80Hz per step in FM and 250Hz in AM for a customizable SW-implemented trimming. In the CGU, all the clock signals used by DSP peripherals are generated from the master clock, and the DSP is allowed to select the clock phase relations and clock frequencies depending on the application.

#### III.b IF Bandpass $\Sigma\Delta$ ADC

The IF-ADC is based on a multi-bit 2<sup>nd</sup>-order  $\Sigma\Delta$  bandpass modulator, as represented in Fig. 4 [10]. It is realized with a switched-cap (SC) technique and it operates at a sampling frequency of 37.05MHz, with a notch frequency at 10.7MHz. The differential input allows 4.0Vpp dynamic range (DR), and it reduces the noise injected back to the tuner. In addition, it provides high rejection to common mode noise. Best performance of the channel equalizer is achieved ensuring up to 65dB IMD linearity; moreover, the minimization of the impulsive current required by the SC input branch is obtained by means of a low-noise switched-buffer. Two self-calibrating control systems ensure in-band noise shaping accuracy. The modulator features 78dB-DR and 72dB peak-SNR considering a 200kHz FM bandwidth, in spite of the noisy environment in which it is embedded.

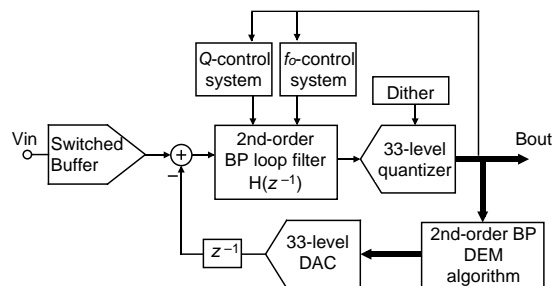


Fig. 4 –Multi-bit bandpass  $\Sigma\Delta$  modulator architecture

#### III.c Tuner AGC Keying DAC

This 8-bit current-steering DAC is used to generate an analog level-signal from the digital processing. This information is sent to the tuner for controlling the Automatic Gain Control (AGC) stage, ensuring the IF-ADC to operate in the linear region.

## IV. Digital Blocks

### IV.a Digital Down Converter

The DDC module computes the in-phase (I) and quadrature (Q) baseband (zero-IF) signals corresponding to the IF input. The 24-bit resolution frequency shift is controllable by the DSP. After the down conversion, the sample rate is 37.05 MHz though the relevant signal bandwidth is few hundreds kHz wide; consequently, a 5<sup>th</sup>-order Sinc filter downsamples data by a 32 factor. An additional decimation is performed by the following two FIR filters, lowering the sample rate to 289.45 kHz. The filter chain is designed to allow 24-bit resolution on the I/Q signals.

### IV.b 24-bit DSP core

The large (148MIPS) computing power makes this device especially suited for sophisticated real-time audio applications. The main features that contribute to the DSP power include:

- **Arithmetic Precision.** The 24-bit data path theoretically allows a dynamic range of 144dB; the 56-bit accumulator, used, for instance, in storing intermediate results in a digital filter, can range over 336dB, highly reducing finite-arithmetic precision errors; moreover scaling and saturation arithmetic is available along with the possibility of having double-precision 48x48-bit multiplications.
- **Debug Interface.** The software debugging is straightforward thanks to the 4 pin debug serial interface that provides full bit-wise control on registers, program and data memory, single-stepping of the program with a 5-word deep program address history FIFO, instruction injection and disassembling of the program memory.
- **Instruction Pipeline.** The 3-stage Fetch-Decode-Execute instruction pipeline is totally transparent, allowing the programmer not to care about latencies, data and instruction exceptions.
- **Branch instructions.** The hardware DO loop and repeat instructions introduce zero overhead; moreover, up to 7 DO loops or 15 interrupts/subroutines nesting combinations are handled by the hardware. Both fast and long interrupt are available with programmable interrupt priorities and masking.
- **Parallelism.** Thanks to the super-Harvard [8] architecture each execution unit, memory and peripheral operates independently and in parallel with other units. The ALU (arithmetic logic unit), AGU (address generate unit), and PCU (program control unit) are parallelized to execute in a single cycle an instruction pre-fetch, a 24-bit multiplication, a 56-bit addition, two 24-bit or a long 48-bit data move, and two address pointer updates in either linear (increment/decrement by 1, by offset), modulo or reverse carry arithmetic.

### IV.c AM/FM Detector

The AM/FM detector is a programmable DSP peripheral used to detect the phase, amplitude and frequency information of the input complex signal (I/Q signals). It can be used to demodulate PM, AM and FM modulated signals. The detection is performed using a high accuracy CORDIC algorithm implemented serially, yielding an efficient high-speed small-area module; four CORDIC cores are available to allow concurrent software calls.

### IV.d Stereo decoder

The fully digital hardware stereo decoder performs the signal processing necessary to decode an FM MPX signal, after the channel equalization. It ensembles pilot tone dependent Mono/Stereo switching as well as stereo-blend and high-cut. Selectable de-emphasis time constant allows using this module for different FM radio receiver standards. Filters for field strength evaluation are realized in hardware, nevertheless, for maximum flexibility, the field strength processing and the noise cancellation are implemented as software on the DSP; this latter has to provide control signals for the soft-mute, stereo-blend, and high-cut.

### IV.e Radio Data System (RDS)

After filtering the over-sampled MPX signal, the 2-PSK demodulator extracts the RDS data-clock, RDS data-signal and the quality information. The subsequent RDS/RBDS decoder packs the bit-stream into blocks of data. This processing also includes error detection and error correction algorithms. In addition, an automatic flywheel control avoids exhausting data exchange between RDS/RBDS processor and the host.

### IV.f Asynchronous Sample-Rate Converter (ASRC)

This hardware module introduces flexibility to the system since it uncorrelates the sample-rate of the DSP to the data rate of an external device, allowing a transparent and effort-free data exchange from the DSP to other external units. There is no need to explicitly configure the input and the output sample rates, thanks to the Digital Ratio Locked Loop in the ASRC.

## V. Main Digital Interfaces

### V.a Serial Audio Interface (SAI)

Two independent SAI modules have been instantiated in the device; each SAI has a Receive and a Transmit channel, and they can be selected to be either master or slave. The bit clocks and word clocks are routed through the pins, so the audio interface can be chosen to be adapted to a large variety of applications. One SAI transmit channel can be connected to the ASRC, thus separating different audio rate domains.

### V.b High-Speed Serial Synchronous Interface (HS3I)

The High Speed Serial Synchronous Interface is a module used to transmit and receive data at high rate (up to 9.25Mbit/s per channel). Typical use of this interface is to exchange data between two TDA7580 chips for tuner-diversity application or to send special control signals to an external antenna switch in an antenna diversity technique [9]. The synchronization clock has a programmable duty cycle, so to reduce in-band harmonics noise.

## VI. Experimental Results

The proposed device has been realized in a 0.18 $\mu$ m CMOS technology, featuring 6 metal levels, metal-metal capacitors and double oxide thickness. The latter makes available both 0.18 $\mu$ m 1.8V and 0.35 $\mu$ m 3.3V MOS transistors. Fig. 5 shows a picture of the device taken at the microscope. The die active area is 15.21mm<sup>2</sup>. In the photo the different parts of the device have been indicated.

Fig. 6 shows the THD at the audio output in presence of a multipath condition versus delay time with and without the equalization (CMA). The x-axis shows the delay time of the reflection, the y-axis the audio distortion in dB. The FM parameters are the following: 98.1MHz, 20dB $\mu$ V RF level, modulation stereo left, 40kHz deviation,

1kHz signal, 5Hz doppler frequency, 88% reflection. Fig. 7 shows the THD at the audio output in presence of a strong multipath condition versus doppler frequency again with and without CMA (98.1MHz, 20dB $\mu$ V RF level, modulation stereo left, 40kHz deviation, 1kHz signal, 7 $\mu$ s delay time, 88% reflection). Fig. 8 shows THD of the audio output in presence of a close adjacent channel with and without the equalization (desired channel: 98.1MHz, 30dB $\mu$ V RF level, modulation mono, 40kHz deviation, 400Hz signal; undesired channel: 98.2MHz, modulation mono, 40kHz deviation, 6.3kHz signal). Fig. 9 shows the THD of the audio output in presence of an alternate channel (desired channel: 98.1MHz, 30dB $\mu$ V RF level, modulation mono, 40kHz deviation, 400Hz signal; undesired channel: 98.3MHz, modulation mono, 75kHz deviation, 6.3kHz signal).

## VII. Acknowledgments

The authors especially wish to thank P. Ruffino for program management, M. Bricchi, J. Henkel, and A. Hoffmann for software design, G. Roither for system definition, S. Galatin and M. Tonella for the applications, F.A. Mancuso, P. Mastromatteo and P. Volontieri for analog layout, and M. Porta for top-level assembly and back-end.

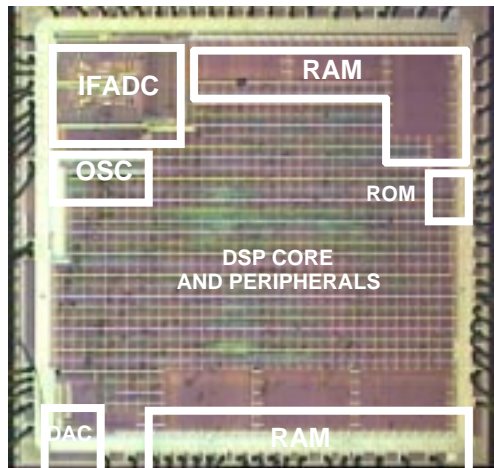


Fig. 5 – Single chip AM/FM receiver chip photograph

## VIII. Reference

- [1] H. van Rumpt, D. Kasperkovitz, J. van der Tang, A Digitally-Programmable Zero External Component FM Radio Receiver with 1 $\mu$ V Sensitivity”, ISSCC2003
- [2] L. Vogt, D. Brookshire, S. Lottholz, G. Zwiehoff, “A two-chip Digital Car Radio”, IEEE Internat. Solid-State Circuits Conference, 1996. Digest of Technical Papers, pp. 350-351
- [3] J.W. Whitehart, “DSP-Based Radio with IF Processing”, SAE Technical Paper Series, 2000-01-0069, presented at SAE 2000 World Congress, Detroit, March 6-9, 2000
- [4] J.E. Volder, The CORDIC Trigonometric Computing technique. IRE Trans. On Electronic Computing, Vol. EC-8, pp. 330-334, Sept 1959
- [5] R.E. Crochiere and L. R. Rabiner, Interpolation and decimation of digital signals – A tutorial Review. Proc. IEEE, Vol. 69, No. 3, pp. 300-331, March 1981
- [6] E.B. Hogenauer, An economical class of digital filters for decimation and interpolation. IEEE trans on acoustic, speech, and signal processing, Vol. ASSP-29, No.2, pp. 155-162, April 1981
- [7] C.R. Johnson, P. Schniter, T.J. Endres, J.D. Behm, D.R. Brown and R.A. Casas, Blind equalization using the constant modulus criterion: A review. Proc. IEEE, pp 1927-1950, October 1998.
- [8] J.L. Hennessy, D.A. Patterson, Computer Architecture: a quantitative approach, Morgan Kaufmann Publishers, 1990.
- [9] L.C. Godara, Applications of Antenna Arrays to Mobile Communications, Part I: Performance Improvement, feasibility and System Considerations. Proc of IEEE, Vol.85, No.7, pp 1031-1242, July 1997.
- [10] V. Colonna, G. Gandolfi, F. Stefani, and A. Baschiroto, “A 10.7MHz Self-Calibrated SC Multibit 2nd-Order Bandpass  $\Sigma\Delta$  Modulator”, European Solid State Circuits Conference (ESSCIRC2002) - Florence (It) - Sept. 2002 - pp.575-578

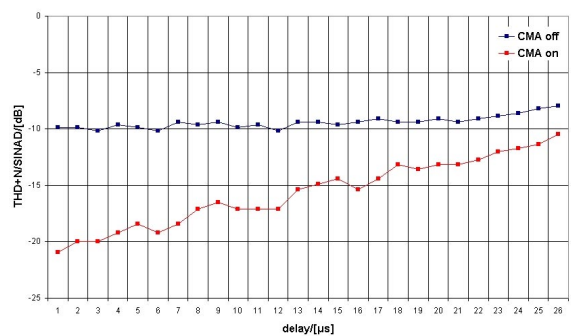


Fig. 6 – THD in multipath condition versus delay time

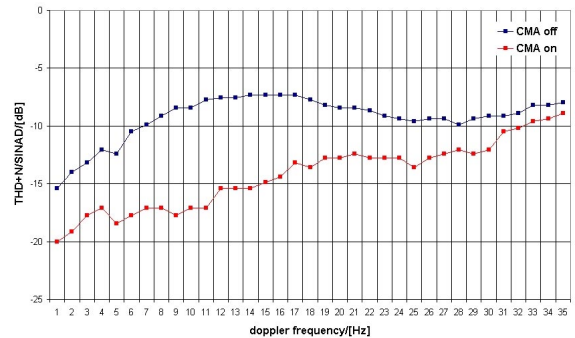


Fig. 7 – THD in multipath condition versus doppler frequency

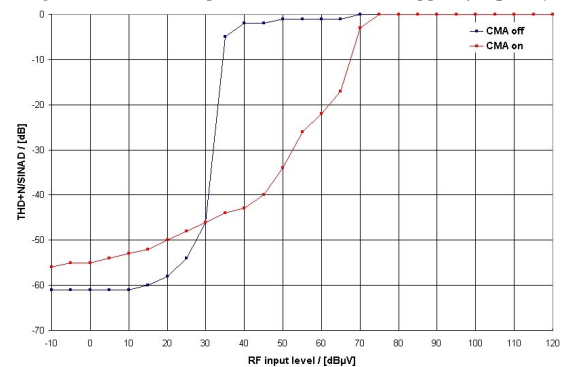


Fig. 8 - THD in adjacent channel condition versus RF level

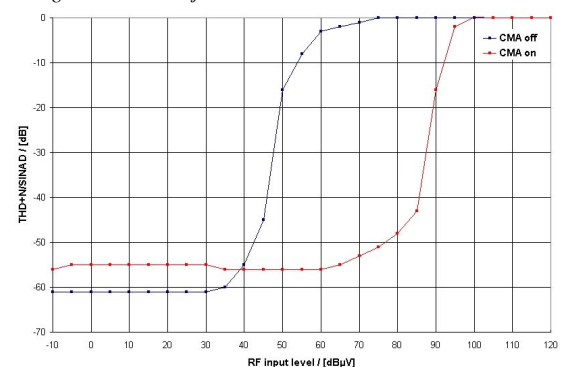


Fig. 9 - THD in alternate channel condition versus RF level

TABLE I – DEVICE SUMMARY

Technology		CMOS
Min. transistor length	$\mu$ m	0.18
Package type		TQFP64
Die area	mm <sup>2</sup>	15.21
Analogue supply	V	3.3
Digital supply	V	1.8
Analogue current consumption	mA	50
Digital current consumption	mA	140
Equivalent kgates*		395
Boot ROM	kbyte	6
Program RAM	kbyte	12
Data RAM	kbyte	18

\*Equivalent kgates are computed using the NAND2 gate area as base-unit without considering memories.