Electrical properties of MOCVD praseodymium oxide based MOS structures

R. Lo Nigro,* R. Toro,# G. Malandrino,# V. Raineri,* and I.L. Fragalà#

* IMM, sezione di Catania, CNR, Stradale Primosole n 50, 95121 Catania, Italy.
#Dipartimento di Scienze Chimiche, Università di Catania, and INSTM, UdR Catania, Viale A. Doria 6, 95125 Catania, Italy.
E-mail: raffaella.lonigro@imm.cnr.it
gmalangrino@dipchi.unict.it
lfragala@dipchi.unict.it

Abstract

Praseodymium oxide-based high k dielectric thin films grown by metal-organic chemical vapour deposition (MOCVD) at 750°C on p-type Si (100) substrate have been proposed. It has been revealed by energy-filtered TEM analyses that depositions in 10^{-3} torr oxygen partial pressure produced Pr_2O_3 and a $Pr_nO_{2n-2}{\cdot}SiO_2$ bottom layer. The electrical properties of both $Pr_2O_3/Pr_nO_{2n-2}{\cdot}SiO_2$ structures and $Pr_nO_{2n-2}{\cdot}SiO_2$ thin layer have been investigated and compared.

1. Introduction

The International technology Roadmap for Semiconductors[1] indicates that new dielectric thin films will be required for future semiconductor technology. In fact, the decrease of SiO_2 gate thickness has reached a level where electrons can directly tunnel through the barrier material, leading to excessive source current drain. The greatest challenge to the continued scaling down of the metal-oxide-semiconductors (MOS) transistor will be the replacement of the SiO_2 gate dielectric with an high k material. New high-k gate dielectric materials are required to increase the effective gate thickness to maintain gate capacitance while reducing the current gate leakage. There is a significant effort currently underway geared toward development of high-k materials for next generation gate dielectrics. In particular, the definition of gate stack and subsequent thermal processing can affect the dielectric thickness and its electrical properties. Therefore, the growth of alternative high k materials on Si substrates attracts more and more attention due to the scientific interest beside the urgent need for gate dielectrics replacements. In particular, the insulator should satisfy requirements such as a high breakdown strength, a low leakage current at operating voltage, a low oxide trap charge, and a high thermal stability on Si[2].

On the other hand, high k materials may also have applications for embedded elements. In fact, on increasing the working frequency in RF circuits passive components, as metal-insulator-metal (MIM) or varactors, the capacitance value needs to become greater. Thus miniaturisation of these devices can be obtained by using giant high k materials or adopting 3D high k structures based on trench technology. For these applications, both the film material type and the semiconductor device geometry will result in the need for advanced chemical vapour deposition processes to produce films.

In this context, the investigated dielectrics include ZrO_2, $ZrSiO_4$, HfO_2, $HfSiO_4$ and among the others, rare earth oxides (REO) form one of the most interesting group for both applications[3-5]. To date, there are only few reports on REO growth using physical deposition techniques. For further progress, a more industry compatible deposition technique, such as metal-organic chemical vapour deposition (MOCVD) is needed. In particular, praseodymium oxide, Pr_2O_3 has a dielectric constant value, k=30, high enough to be considered as an alternative dielectric on silicon substrates. In addition, Pr_2O_3 has a relatively high band gap, of about 3.9 eV and a high formation energy. Some reports on MBE deposited Pr_2O_3 films demonstrated low equivalent oxide thickness (EOT), low leakage, and good reliability characteristics[6,7]. Recently Pr_2O_3 films have been deposited using the MOCVD technique[8]. Further motivation for the study of the Pr_2O_3/Si(100) system has been provided by the fact that preliminary electrical charaterization of MOCVD polycrystalline Pr_2O_3 films has produced good results. However, electrical properties of praseodymium oxide based films have not been reported to the best of our knowledge. This paper reports on the electrical characterization of MOCVD synthesised praseodymium oxide based films by comparison of different film thicknesses suitable for MIM and MOS devices, respectively.

2. Experimental

Pr_2O_3 films having different thicknesses were deposited from the $Pr(tmhd)_3$ [(H-tmhd=2,2,6,6-tetramethylheptane-3,5-dione)] precursor in a hot wall reduced pressure MOCVD reactor. Substrates of p-type Si(100) wafer with resistivity of 5 m? c m^{-1} and with an

epy-layer having resistivity of 20 ? cm^{-1} were used. Their surface was treated with dilute HF to remove the native oxide, and successively rinsed with acetone and isopropanol. Film growth occurred at 750°C using an Ar flow as carrier gas under an oxygen partial pressure as low as 10^{-3} torr. Microstructure and morphology were investigated by cross-sectional transmission electron microscopy [(Field emission gun-transmission electron microscope) FEG-TEM JEOL 2010F] equipped with the Gatan imagining filter (GIF) has been used.
Finally, the chemical compositional of interfaces were carried out by energy filtered-TEM analyses [(FEG-TEM JEOL 2010F equipped with the Gatan imagining filter (GIF)].
Metal-oxide–semiconductors (MOS) (Au/Pr-based films/p-Si/Au) structures having several radius ranging from 50 µm to 170 µm have been fabricated. Current density-voltage (J-V) characteristics were measured by the semiconductor parameter analyzer (HP4156B) and capacitance-voltage (C-V) characteristics were measured at 1 MHz in a low noise probe station using C-V plotters (HP4284A).

3. Results

In the bright field TEM cross section image (figure 1a) of a praseodymium oxide thin film grown for 45 minutes, a bottom layer few nm thick and a top layer of about 85.5 nm, both having the same contrast, are present. The interface structure has been better investigated by High-resolution TEM image (figure 1b) and it consists of an SiO_2 layer, an bottom praseodymium oxide based layer, about 8 nm thick, having no long range order, and an ordered region of Pr_2O_3 grains. The crystallographic structure of the deposited films has been studied by electron diffraction pattern. The distribution of spots on circles having diameters of 3.34, 3.02, 2.94, 2.24, 1.94 and 1.72, can be unambiguously assigned to the (100), (002), (101), (102), (110), and (103) reflections of the hexagonal polycrystalline Pr_2O_3 phase.

On the other hand, praseodymium oxide-based films grown for 10 minutes consists of a 9.8 nm layer having the same morphology of the bottom layer found in the Pr_2O_3 films. The electron diffraction pattern of this layer suggests an amorphous nature. Its chemical composition has been investigated by energy filtered transmission electron microscopy (EF-TEM) analysis using the three windows method. This represents an innovative technique to study chemical composition and film/substrate interface in a non-destructive way by recording bidimensional chemical maps with high spatial resolution and sensitivity (˜ 5%). The chemical map images and relative profiles point to a non zero Si concentration indicating the formation of a Pr_nO_{2n-2} •SiO_2 layer. The formation of multiple layer stacks consisting of REO/RESiO/SiO_2, where RE is an element of rare earths, has been already observed for other RE elements such as Y and La, in both physical vapour deposition (PVD) and chemical vapour deposition (CVD) processes.

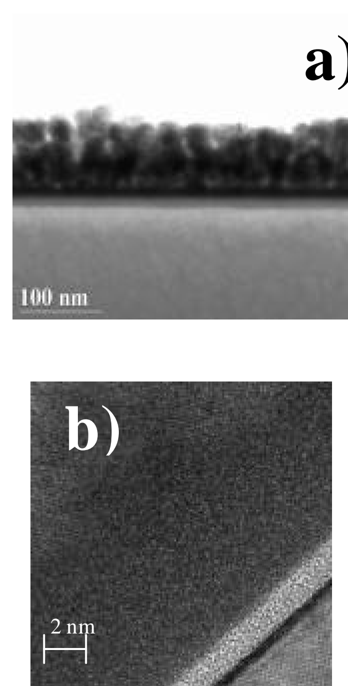

Figure 1. a) Low-magnification bright field TEM image of praseodymium oxide films grown for 45 minutes at 750°C and **b)** the relative High-resolution TEM image of the praseodymium oxide film/substrate interface.

Electrical characteristics of the dielectric consisting of both Pr_2O_3 films and Pr_nO_{2n-2}·SiO_2 thin layer having 93.5 nm and 9.8 nm thickness, respectively, have been investigated by capacitance-voltage (C-V) and current–voltage (I-V) analysis. Au-gate MOS capacitors with an active area ranging from 7.85×10^{-5} cm^2 to 9.07×10^{-4} cm^2 were fabricated on p-type (100) Si substrate (5 mΩ cm^{-1}) with a p-type epi-layer of 20 Ω cm^{-1}. Au was sputter-deposited, patterned and wet-etched to form the top electrode. In particular, a I_2/2I$^-$ solution was used to selectively remove the gold layer after resist patterning. The complete gold removal was optically evaluated, while the Pr_2O_3 surface roughness and morphology, analyzed after etching, resulted identical to the as-deposited film, i.e no surface damage was detected after etching by atomic force microscopy. The film thickness did not change after etching, too. Resist removal was obtained by acetone. The back contact was formed by Au metal sputtering on the low resistivity substrate, after native oxide removal. The C-V characteristics of two films 93.5 nm and 9.8 nm thick have been measured both at 1 MHz for comparison. The MOS capacitors are biased at inversion driven to accumulation and then back to inversion, with a sweep rate of 0.2 V/sec.
In the case of 93.5 nm thick film (figure 2a), the limited hysteresis of about 70 mV has been observed. As the Au gate voltage has been decreased to more negative values, the majority charge carriers (holes in the p-type Si substrate) have been accumulate near the interface and early saturated. The same behavior is observed in

inversion as the gate voltage becomes increasingly positive which means that the various Pr_2O_3 mobile charges are negligible.

The flat band voltage is of about 1 eV considering also the shift due to the built +p voltage at the epi-substrate junction. The capacitance value in accumulation capacitance was used to determine the effective dielectric constant. The dielectric constant (ε) value of the Pr_2O_3 films has been calculated to be about 26.

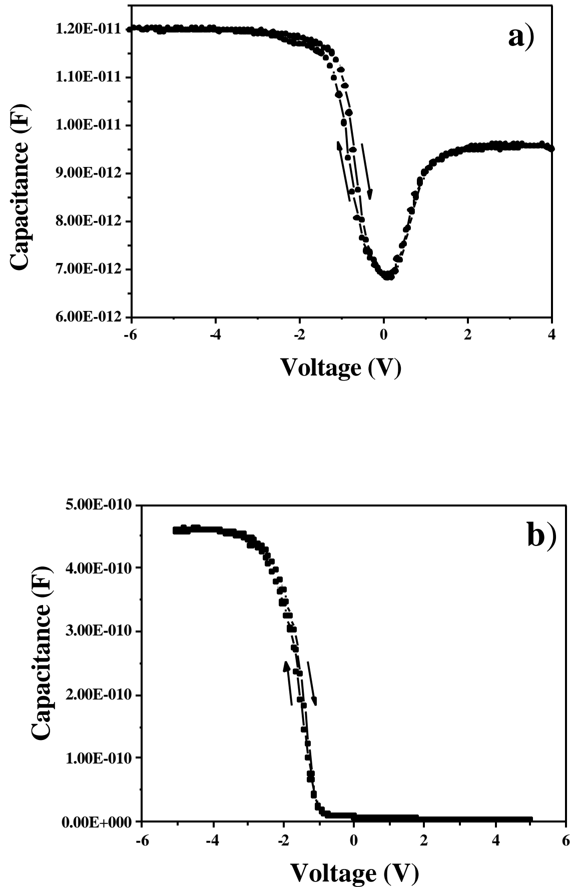

Figure 2. C-V curves of Au/dielectric/ Si capacitors, where dielectric layer is a 93.5 nm Pr_2O_3 film **(a)** and a 9.8 nm $Pr_nO_{2n-2}{\cdot}SiO_2$ film **(b)**. The capacitance has been measured at 1 MHz under forward and reverse biases.

The results obtained from high frequency (1 MHz) C-V characteristics of a typical MOS device with a 9.8 nm thick dielectric layer is plotted in figure 2b. The sample also shows an almost negligibly small hysteresis of about 15mV having parallel behaviour. In high-k materials hysteresis is commonly observed in C-V characteristics and hysteresis minimization is required for the high k materials to be utilized in memory applications. The curves in figures 2a and 2b show a "clockwise" hysteresis, indicating the movement of a net negative charge (electrons) in the insulator during the measurements. This behaviour can be attributed to electron injection from the gate, when the devices is biased at accumulation and subsequent trapping into the dielectric. The fact that during subsequent sweeps the same hysteresis characteristics (both in magnitude and type) are obtained, indicates that electron trapping occurs at relatively shallow trapping sites. It should be noted that positive (holes) injection from the semiconductors may be prohibited due to interfacial SiOx layer typically formed in the reactor chamber during heating at 750°C deposition temperature.

The C-V characteristics are directly related to the charge defects in the insulator and at the insulator/semiconductor interface. The unbalanced charges arising from defects will cause a C-V curve shift. The C-V curve in figure 2b exhibits a larger shift in V_{fb} with respect to the one observed in the C-V curve of figure 2a indicating a larger quantities of fixed charges in the thinner film with respect to the thicker dielectric system. The shift increase is likely caused by positive charges due to oxygen vacancies, which may arise from oxygen deficiency as well as dangling bonds present at the interface.

By directly convertion of the areal capacitance, C, measured for the thinner film, the relative dielectric constant has been estimated to be 7.6.

The leakage current densities of both films as a function of the applied gate bias V are shown in figures 3a and 3b. Each measurement starts from positive values (forward sweep) with a voltage step of 0.1-0.2 V/sec.

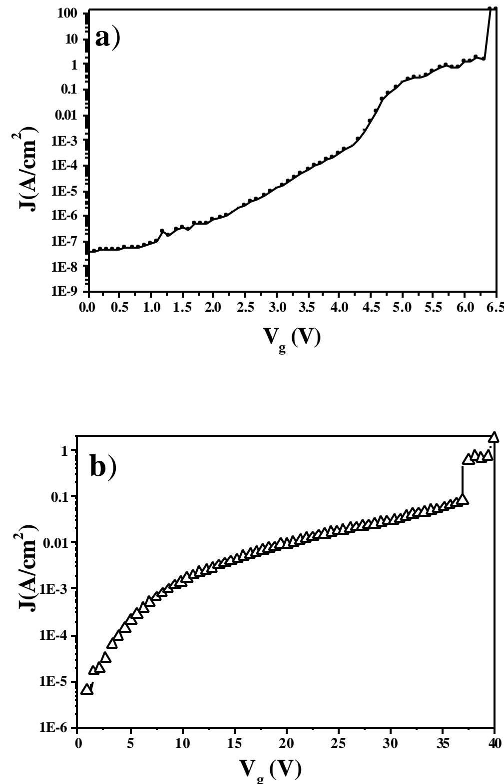

Figure 3. I.V curves for the 93.5 nm **(a)** and 9.8 nm **(b)** samples, respectively. The leakage current densities measured at +1V are 8.3x 10^{-8} A/cm^2 for the 93.5 nm thick dielectric and 6.5x 10^{-6} A/cm^2 for the 9.8 nm thick dielectric.

For the case of the 93.5 nm thick dielectric MOS capacitors, figure 3a shows the leakage current characteristics in the range from 0 to +7V. The Pr_2O_3 films have shown a low leakage current density of about 8.3x 10^{-8} A/cm^2 at +1V.

For the 9.8 nm thick dielectric layer, the leakage current density as a function of the applied gate bias V is shown in figure 3b. The leakage current densities in accumulation is J (+1 V) =6.5x10^{-6} A /cm^2. At a +1V accumulation bias the leakage current density increases less than a factor 3 by decreasing the thickness of a factor 10.

The present electrical measurements indicate that in the case of praseodymium silicate thin layer, the measured dielectric constant value is not fairly impressive. However, note that both dielectric constant and leakage current density at +1V are not so different from the reported values for REO/RE silicates systems[9,10].

Moreover, we emphasize that these results were obtained with no post-processing after annealing, which generally is used to improve the interface characteristics and properties. Finally, the electrical measurements presently reported represent a preliminar step to the understanding of the deposition chemistry of the praseodymium based films which can not be deducted by the incomplete thermodynamic information[11]. Further studies are underway to test annealing effects, influence of deposition temperatures on the interlayer formation, and the compatibility with the poly-Si gate.

4. Conclusion

In summary, praseodymium oxide films have been grown on Si(100) substrates by MOCVD. TEM diffraction measurements point to random Pr_2O_3 thin film, and differences of the microstructure between film and interface have been observed. A bottom oxygen rich layer is present whose crystallographic/morphological nature was defined as a Pr_nO_{2n-2}/SiO_2 layer by energy-filtered analyses.

Polycrystalline 93.5 nm thick Pr_2O_3 films have shown a dielectric constant of about 26 and leakage current densities of 8.3x 10^{-8} A/cm^2 at +1V, with a negligible hysteresis in the C-V curves. At a +1 V accumulation bias the leakage current density increase by a factor 2 by decreasing the thickness of a factor.

Leakage currents were found to decrease by two orders of magnitude by decreasing the thickness of a factor 10. The C-V curves of 9.8 nm Pr_nO_{2n-2}/SiO_2 samples show a dielectric constant of 7.6. We emphasize that these results were obtained with no post-processing after annealing. In addition, MOCVD growth of REOs would enable new application of these materials, for example for trench or MIM capacities and the electrical properties of praseodymium oxide based capacitors have motivated us to probe the details of the deposition chemistry.

5. References

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