

# A 16-bit 60 $\mu$ W Multi-Bit $\Sigma\Delta$ Modulator for Portable ECG Applications

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## Abstract

To address the growing field of on-line, out-of-hospital health care a front-end ADC for portable electrocardiographic systems has been designed. The converter is realized as a first-order, 3-bit  $\Sigma\Delta$  with an oversampling ratio of 512. Performance is optimized to adhere to the standard IEC60601-2-47, which governs ambulatory ECG equipment. The single ended design achieves a dynamic range of 16 bits for signal offsets up to  $\pm 1.25$  V. Measured power consumption is 60  $\mu$ W with supplies of 2.6 V analog and 2.2 V digital.

## 1. Introduction

The field of on-line, out-of-hospital health care and health supervision is constantly expanding. Shorter or no hospital time for patients could yield large economical savings, and the area receives attention both in medical and technical conferences and journals. Advances in technology and miniaturization of electronics have increased the number of portable, battery-operated equipment available. This is also the case for electrocardiographic (ECG) systems [1, 2], making them available not only for clinical use but also for monitoring in sports or other activities. In these cases, the complete equipment is portable and carried by the patient.

This type of ECG equipment is defined in the standard IEC60601-2-47 [3], which among others sets the performance requirements on the equipment. The required bandwidth of the ECG sensor is low. At the same time, the signal is of low amplitude with large DC offsets, which requires a high dynamic range of the system. Further, if the equipment is to be battery operated and affordable, also power consumption and chip area are important constraints.

One main part in the ECG system is the analog front end, which is decisive for the performance of the equipment. The combination of high resolution, low bandwidth, and low power consumption is well suited to be implemented in a sigma-delta ( $\Sigma\Delta$ ) converter [4]. This paper describes the design of a single channel  $\Sigma\Delta$  converter which together with a preamplifier will adhere to IEC60601-2-47. The converter is intended to be one block in future low-power portable multi-channel ECG equipment.

## 2. Architecture level design

Several standard methods for ECG monitoring exist, [5]. One subset used for a three lead ECG is the Goldberger scheme. In this, virtual ground is created through a star coupled resistive network. The three channels are thereafter measured with respect to this common node. As the Goldberger ECG monitoring scheme is inherently single-ended, a fully single-ended design structure was chosen for the  $\Sigma\Delta$  converter. Going to differential would increase noise immunity, but also increase chip area and power consumption. It was judged that the target resolution could be met with a single ended design in the low frequency range desired.

The following is a subset of the IEC specifications relevant for the initial design of the A/D converter:

- *Noise.* Input referred noise should not exceed 50  $\mu$ V<sub>p-p</sub> over 9 out of 10 periods of 10 s length.
- *Frequency response.* The equipment should have bandpass characteristic with 3 dB roll off at 0.67 Hz and 40 Hz.
- *Minimum feature size.* A 10 Hz, 50  $\mu$ V<sub>p-p</sub> signal shall yield a visual recorded deflection.
- *Input dynamic range.* A 6 mV<sub>p-p</sub> signal shall be measured with offsets up to  $\pm 300$  mV.

The target nominal supply voltage was set to 2.4 V with references at  $\pm 1.2$  V relative to midpoint. That means that a preamplification of the input signal can be used to better utilize the dynamic range of the system. An amplification factor of 3 was chosen, yielding a maximum specified input offset of 900 mV.

For the amplified minimum feature size of 150  $\mu$ V<sub>p-p</sub> the target was that three LSB steps should toggle. This requires an effective LSB for the converter of 50  $\mu$ V. To put safety margin in the design process, a factor of two is included to make the design target value about 25  $\mu$ V per LSB. This gives a quantization noise level of 7.2  $\mu$ V<sub>RMS</sub>. If all other noise sources in the circuit are kept below this value, the IEC specification should be fulfilled.

An LSB of 25  $\mu$ V means a required resolution of 16.5 bits. This can be fulfilled with a number of various structures for a  $\Sigma\Delta$  converter. As the ECG signals are overlaid with large offsets, one requirement is that the resolution is kept even when the signal offset approaches the

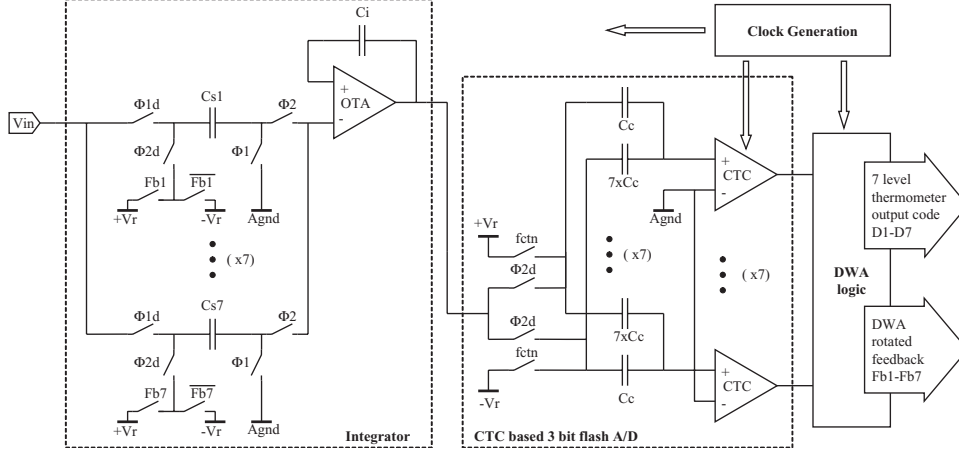


Figure 1. System level schematic showing the four main blocks with relevant capacitors and switches.

references. This implies the use of a multibit converter, as a single bit converter reaches overload in the integrators when exposed to high DC offsets. Further, the amplitude of one feedback step is smaller than the reference voltage in a multibit  $\Sigma\Delta$ . This relaxes the slew-rate requirements on the operational amplifier in the integrator, and allows for lower bias currents than in a single bit design.

First and second order were considered for the modulator structure. Higher orders were not considered due to the increased circuit complexity. For example, either a 3-bit first order modulator with an oversampling ratio of 512, or a 4-bit second order modulator with an oversampling ratio of 32 would fulfil the requirements. The target bandwidth was set at 45 Hz for an equivalent Nyquist sampling rate of 90Hz. The sampling frequencies for the first and second order modulator would be 46.08 kHz and 2.88 kHz respectively. A sampling frequency of 2.88 kHz would mean an approximate hold time for the sampling capacitors of 170  $\mu$ s. With both capacitors and leakage currents in the same order of magnitude (pF, pA), this could give significant voltage drops due to leakage. Also, a second order modulator would require double operational amplifiers, integration capacitors and feedback capacitors. This would increase the chip area needed. Finally, the  $kT/C$  noise from the integrator capacitor would be a factor of four higher for the sampling rate of 2.88 kHz than for 46.08 kHz. With this, the final choice of architecture was set to a first order, 3-bit modulator with an oversampling ratio of 512 times.

### 3. Circuit design

The design is based on four main blocks as shown in the system level schematic in figure 1. The remainder of this section briefly describes the design choices made for these blocks.

The integrator with multibit feedback is built around a single ended Operational Transconductance Amplifier (OTA). The multibit structure and the low sampling frequency give relaxed demands on the OTA, allowing the

use of a standard two stage Miller design. The DAC in the feedback loop is implemented by splitting up the sampling capacitance in 7 equal 600 fF units,  $Cs1$  through  $Cs7$ . Each of these consist of four symmetrically arranged 150 fF capacitors. Layout is optimized to improve matching, with the use of dummy capacitors on edges and full symmetry in the layout of the capacitor array. The equivalent input noise from the sampling capacitors is

$$V_{NRMS} = \sqrt{\frac{kT}{M \sum_n C_{Sn}}} \quad (1)$$

where  $M$  is the oversampling ratio. This yields a noise of 1.4  $\mu$ V<sub>RMS</sub>, giving an acceptable margin to the estimated quantization noise of 7.2  $\mu$ V<sub>RMS</sub>. Although this theoretically would allow for a decrease in capacitor sizes, concerns over matching, charge injection and clock feedthrough set the choice to 600 fF. The input signal is sampled to all sampling capacitors, after which they are connected to  $\pm V_{REF}$ , depending on the digital output value from the flash ADC. The integration capacitor  $Ci$  is equal to the sum of the sampling capacitors, 4.2 pF, giving a gain of one in the integrator.

Power consumption was a key factor in the choice of structure for the A/D converter. Literature search showed a charge transfer comparator (CTC) to be a promising candidate [6, 7]. The circuit consumes no static power, giving very low power consumption for low frequencies. The offset voltage distribution for low frequencies has a sigma less than 1 mV. The influence of offsets in an A/D converter inside a multibit  $\Sigma\Delta$  modulator has been investigated in [8]. Based on these findings the conclusion was drawn that the CTC offset would not be a performance limiting factor. To keep the ADC static power at a minimum, the reference voltage is created using a capacitive ladder in which the unit capacitor  $Cc$  is set to 300 fF.

The use of the CTC based flash converter requires a fairly complicated clock generation. Thus, the main input clock had to be set to 8 times the sampling frequency. From the main clock the various phases for the CTCs as

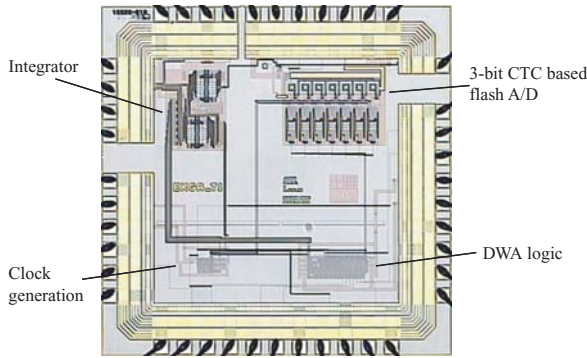


Figure 2. Chip photograph.

well as the non-overlapping clocks for the integrator are derived.

Multibit  $\Sigma\Delta$  converters are sensitive to non-idealities such as mismatch in the feedback D/A converter, as these errors are added directly to the input signal and are thus not noise shaped. For target resolutions exceeding the matching possibilities in CMOS this problem must be addressed. One technique is to use Data-Weighted Averaging (DWA), [9]. The implementation chosen here selects the unit elements used in the D/A conversion sequentially, always starting with the next unused element. Ideally, this translates mismatch into high frequency noise. However, when the input to the converter is periodic, the mismatch can translate into tones in the converter baseband spectrum. As discussed below in section 4 this behavior was found to slightly reduce the performance of the implemented modulator. Several ways to address the tone behavior exist [10], and will be addressed in the next revision of the circuit.

The chip was built in the Austria Micro Systems 0.35  $\mu\text{m}$  CMOS process, which allows the use of double poly capacitors. Care was taken to separate analog and digital parts on chip. All four main blocks and the digital pad drivers have separate supplies, to allow measurements of power consumption for each block. A chip photograph outlining the four main blocks is shown in figure 2.

#### 4. Measurements

The chip was bonded in a CLCC44 package and attached to a test circuit board. Analog power supply and references were supplied from separate battery packs using NiMH accumulators. This set the analog supply voltage at 2.6 V and references at  $\pm 1.3$  V relative to analog ground at 1.3 V. Digital supply was taken from a power supply set to 2.2 V. Sampling frequency used was 46 kHz. The 368 kHz main clock was brought on board single ended, with an amplitude of 2.2 V. Recorded output data length was 128 kword. All signal processing was made in Matlab. As the structure of the digital filter was not yet decided, the noise energy was integrated up to the Nyquist bandwidth of 45 Hz. This means that performance with a

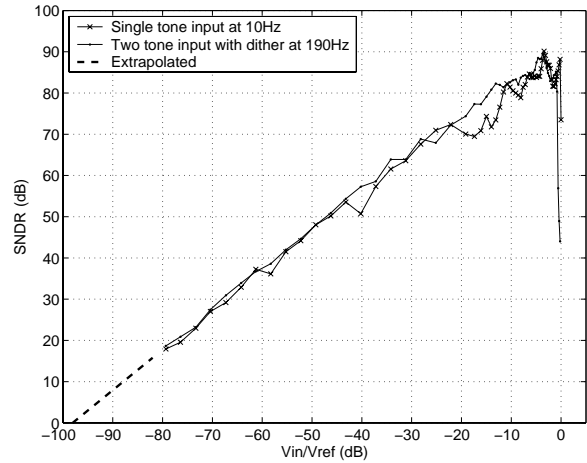


Figure 3. Measured SNDR vs. input amplitude with and w/o dither signal applied.

real filter will be reduced, the amount of which depends on the chosen filter structure.

The measured SNDR as a function of input amplitude is shown in figure 3. Initially the measurement was performed using a single tone 10 Hz input signal. It was then seen that the performance was limited at certain amplitudes by tones in the baseband, generated by the DWA. To test the effect of a dither signal, an out of baseband tone at 190 Hz with an amplitude of 0.14 V was added to the 10 Hz signal. This shifted the tones outside the baseband and a much smoother curve was recorded. From these measurements a maximum SNDR of 90 dB was recorded. The dynamic range (DR) indicated is 98 dB, equivalent to 16 bit resolution.

The influence of varying oversampling ratio on the DR was measured by adjustment of the bandwidth to give different oversampling ratios, figure 4. The sampling frequency was kept at 46 kHz. The measurement shows that the converter comes very close to achieving quantization

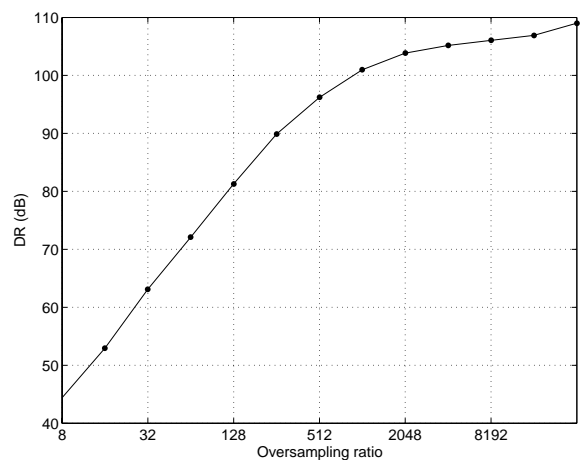


Figure 4. Measured dynamic range vs. oversampling ratio.

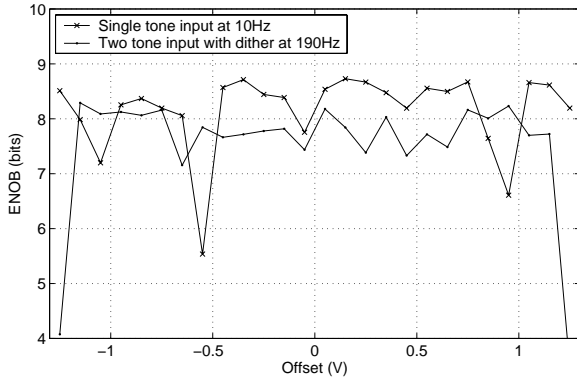


Figure 5. Measured ENOB for a  $4\text{ mV}_{RMS}$  10Hz input signal vs various DC offsets.

noise limitation up to the target oversampling ratio of 512. The DR increases 1.5 bit per octave as expected for a first order modulator up to an oversampling ratio of 256. For the next doubling the increase is slightly smaller, dropping off to be 0.5 bit per octave which indicates that the limitation then is other noise sources. As the design margin for the  $1/f$  noise in the OTA was fairly low, this could be a limiting factor. Also injection of digital noise is a strong contributor. Nevertheless, also this measurement shows a DR of close to 16 bit.

To verify the required performance with high DC offsets on the signal, a  $4\text{ mV}_{RMS}$  signal was applied with various offsets levels. The measured data are shown in figure 5. Also in this measurement the performance was limited at certain input amplitudes by tones in the baseband. The same measurement was performed with a dither signal applied. This stabilizes the performance, even though the maximal ENOB is slightly reduced. From the graph it can be seen that the performance is kept with offsets very close to  $\pm V_{REF}$ . With an applied dither the drop off comes earlier as the dither adds signal amplitude.

Table 1. Specifications and measured performance.

Dynamic Range	98 dB
SNDR	90 dB
Nyquist Bandwidth	45 Hz
Clock Frequency	368 kHz
Sampling Frequency	46 kHz
Oversampling Ratio	512
Reference Voltage	$\pm 1.3\text{ V}$
Input offset tolerance	$\pm 1.25\text{ V}$
Supply Voltage Analog	2.6 V
Supply Voltage Digital	2.2 V
Power Consumption	$60\ \mu\text{W}$
Technology	$0.35\ \mu\text{m}$ CMOS TMDP
Active Silicon Area	$0.7\ \text{mm}^2$

Finally the power consumption for the various parts of the chip was measured. The total power consumption was  $60\ \mu\text{W}$ , divided into  $47\ \mu\text{W}$  for analog supply,  $3\ \mu\text{W}$  for reference voltages and  $10\ \mu\text{W}$  for digital supply. The measurements results are summarized in table 1.

Preliminary measurements were also made running the chip at a sampling frequency of 256 kHz for a Nyquist bandwidth of 250 Hz, as this is a requirement for clinical ECG monitoring. These measurements show similar performance as those discussed above, with the total power consumption increased to  $185\ \mu\text{W}$ .

## 5. Conclusions and further work

The design of a  $\Sigma\Delta$  ADC optimized for portable ECG equipment has been presented. The converter is realized as a first-order, 3-bit  $\Sigma\Delta$  with an oversampling ratio of 512. Measured performance includes a dynamic range of 16 bits for signal offsets up to  $\pm 1.25\text{ V}$  with a power consumption of  $60\ \mu\text{W}$ . Future work will involve a re-design of the DWA logic to alleviate tones in the baseband. Also, a complete low-power 3-channel ECG chip including preamplifiers and digital filtering will be built based on the presented work.

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