A 1.8 GHz CMOS $\Delta\Sigma$ Fractional-N Synthesizer

Bram De Muer and Michiel Steyaert
ESAT - MICAS K.U. Leuven,
Kasteelpark Arenberg 10, B-3001 Heverlee
demuer,steyaert@esat.kuleuven.ac.be

Abstract

A 1.8 GHz $\Delta\Sigma$ fractional-N frequency synthesizer is presented. The digital synthesizer part is integrated together with an LC- VCO, a 35 kHz dual-path loop filter and a 16 modulus prescaler in 0.25μm CMOS technology. The zero-dead zone phase detector is optimized towards linearity and spurious suppression. The influence of MASH and multi-bit, single-loop $\Delta\Sigma$ modulators on the synthesizer performance is simulated and experimentally verified. The synthesizer consumes 35 mA from a single 2 V power supply, 25 mA of which is due to the integrated VCO. The measured phase noise is lower than -120 dBc/Hz at 600 kHz. Reference spurs are below -75 dBc, while the fractional spur level is lower than -100 dBc.

1. Introduction

Driven by economical forces, the consumer telecom market has pushed the telecommunication system designers to smaller and cheaper solutions. Integration of the analog RF part of wireless transceivers in cheap digital CMOS technology seems a viable solution. A major challenge in the design of future CMOS single-chip transceivers is the frequency synthesizer. The most popular synthesizer type is the Phase Locked Loop (PLL). Techniques have been presented to improve the overall performance of PLLs, the most promising of which is $\Delta\Sigma$ fractional-N synthesis [1] (Fig. 1). The $\Delta\Sigma$ fractional synthesis technique enables fine frequency resolution with a high reference frequency by employing fractional division. Therefore higher loop bandwidths can be chosen, alleviating the speed-resolution trade-off of integer-N PLLs. The energy of spurious tones that emerge from the fractional division, is randomized and pushed to higher frequencies by a noise shaping $\Delta\Sigma$ modulator.

This paper presents a 1.8 GHz $\Delta\Sigma$ fractional-N frequency synthesizer, integrated in a 0.25μm CMOS technology. First, the design of the PLL is discussed, focusing on minimizing the integrated loop filter capacitance while maximizing the phase noise performance and on Phase-Frequency Detector (PFD) linearity. The next section presents the simulation of the fractional spur generation and noise folding due to non-linearities present in the PLL, especially the PFD-charge-pump non-linearity. To conclude, experimental results with different $\Delta\Sigma$ modulators are presented.

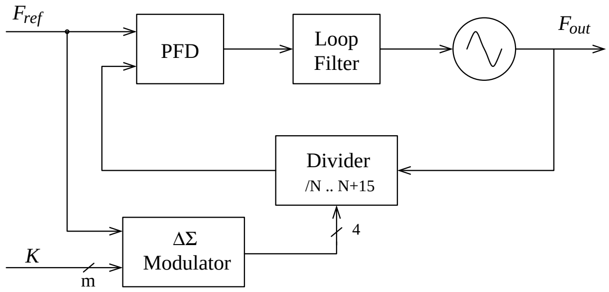

Figure 1. The principle of $\Delta\Sigma$ fractional-N synthesis

2. The Phase Locked Loop

A 4-th order, type-II PLL is integrated, including a 64/79 prescaler, a zero-dead-zone PFD, a dual charge-pump and a 3-step equalizer together with the LC-tank VCO and a third-order, 35 kHz low-pass loop filter (see Fig. 2).

2.1. The 64/79 prescaler

The high-speed division of the prescaler is done with two DSTC n-latches [2], forming a differential dynamic D-flipflop. The flipflop operates with rail-to-rail internal signals to minimize the residual prescaler phase noise. The 16-modulus division (64..79) is implemented with the phase-switching topology [3]. The different divide factors are generated by switching between the 90^o spaced output phases of the second flipflop. When the 90^o spacing is not ideal, spurs can be generated at 1/4, 2/4 and 3/4 of the PLL reference frequency. By careful layout and circuit design, the spurs are suppressed to negligable levels. The maximum operating frequency of the prescaler is 2.2 GHz for 11 mW.

2.2. The LC-VCO

The parasitic resistance of the integrated coil is crucial for the out-of-band phase noise of the PLL. Using an inductor simulator-optimizer, the inductor Q is pushed to 9 for a standard CMOS process with 2 metal layers (0.6 mm and 1.0 mm) and a substrate resistance of 5 Ω cm. The measured phase noise is as low as -127.5 dBc/Hz at 600 kHz. For the VCO gain cell, only PMOS transistors are implemented, to maximize the useful voltage range for tuning, resulting in a tuning range of 28% [4]. The VCO output is buffered from the prescaler input to prevent kick-back noise entering the LC-tank.

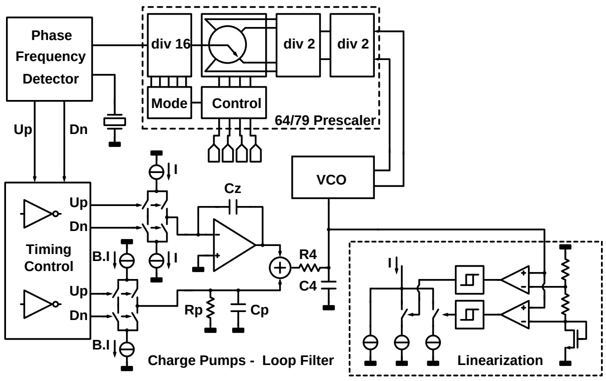

Figure 2. The 4th-order, type-II dual-path PLL

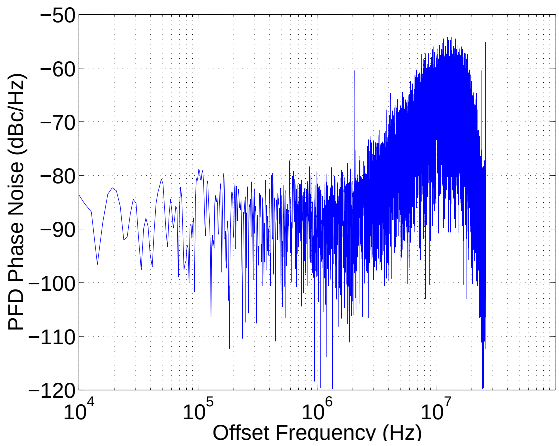

Figure 3. The simulated PFD output spectrum with PFD non-linearities (5% gain mismatch and 1% dead zone)

2.3. The dual-path loop filter

To achieve full integration, a dual-path filter topology has been implemented (Fig. 2). Two filter paths, one integration (C_z) and one low-pass filter (C_p, R_p) are added to reveal the zero, needed for loop stability in a type-II PLL, without additional capacitance [3]. An extra pole (C_4, R_4) is added to ensure enough suppression at higher offset frequencies. The total number of capacitors is the same as in a classical 4th-order, type-II PLL, but for the same phase noise the integrated capacitance is more than 5 times smaller (only 1.4 nF). The resulting loop bandwidth is 35 kHz, the phase margin is 57^o and the damping ζ is 0.77.

2.4. The PFD and charge pump

The reference spur generation by the PFD-charge-pump circuit, is carefully minimized. The integration in the first path of the loop filter is done actively to keep the charge pump output at a fixed level . Secondly, the charge pump current is designed to be at least a magnitude larger than the fixed parasitic charge injection of the switch transistors. The current switches are implemented with PMOS and NMOS transistors to compensate charge injection. Last but not least, a timing control scheme (Fig. 2) is developed to control the charge-pump switches. As a result, undesired charge is not injected in the filter impedance, but is deviated through dummy current branches and hard on/off switching of the current sources is prevented. consists of invertors and latches. The invertors provide the delay between the actual and the dummy current branche. The latches synchronize the signals for the actual current branche.

Since the PLL is intended for $\Delta\Sigma$ fractional synthesis, the linearity of the PFD-charge-pump circuit is crucial. First of all, the phase detection is performed by a zero-dead-zone PFD [5], to prevent hard non-linearities around 0^o phase error. Secondly, the current source transistors are oversized to ensure sufficient matching, such that the gains for positive and negative phase error detection are equal. Thirdly, the timing control provides synchronization between the two filter paths and the switches of the charge pumps themselves, again ensuring equal phase error detection gain.

3. $\Delta\Sigma$ Fractional-N Synthesizer

3.1. Theoretical analysis

A block diagram of a $\Delta\Sigma$ fractional-N synthesizer is shown in Fig. 1. The $\Delta\Sigma$ modulator output is on average $K/2^m$ cycles of the reference frequency F_{ref}. The resulting output frequency is then $F_{out} = N + K/2^m$. The $\Delta\Sigma$ modulator randomizes spurious energy to high frequency noise, which is removed by the averaging in the loop filter. The ratio between the loop bandwidth and the sampling frequency should be larger than 100 to ensure enough filtering of the low-frequency quantization noise [6].

Although fractional-N synthesis lowers the necessary division modulus and thus the in-band phase noise multiplication, the modulator will also contributes to the overall phase noise. To model the impact of $\Delta\Sigma$ control, a LTI model can be used. The prescaler-modulator combination can be seen as a digital-to-phase (D/P) converter, which subtracts 0 or $n * 2\pi$ rad every reference cycle, with $n = 0..2^4$. The prescaler modulus is then given by (1) with $H_{qnoise}(z)$ the noise shaping function and $Q(z)$ the quantization noise, with a PSD of $1/(12.F_{ref})$ under the assumption of white noise.

$$N(z) = N + \frac{K}{2^m} + H_{qnoise}(z).Q(z) \qquad (1)$$

$$F_{out} = \left(N + \frac{K}{2^m}\right).F_{ref} + H_{qnoise}(z).Q(z).F_{ref} \qquad (2)$$

By integrating the PSD of the frequency fluctuations, the phase noise at the output of the prescaler is found (3):

$$S_\Theta(z) = \frac{\pi^2}{3.F_{ref}}.\frac{|H_{qnoise}(z)|^2}{|1 - z^{-1}|^2} \qquad (3)$$

The results of theoretical analysis are shown as lines in Fig. 4.

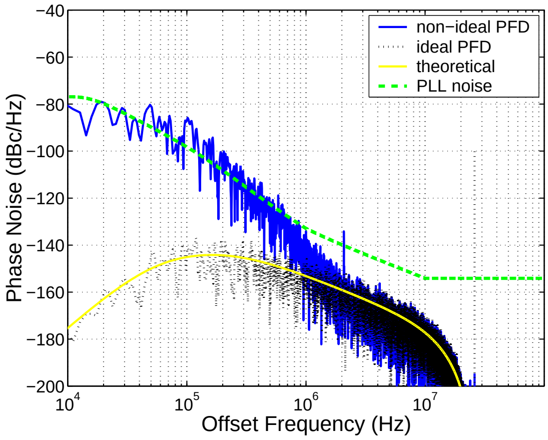

Figure 4. The simulated fractional-N PLL output spectrum with and without PFD non-linearities compared with the integer-N output

3.2. Non-linear analysis

As can be seen in Fig. 4, the linear analysis cannot reproduce noise folding and spur generation. Therefore, a non-linear simulation method is developed that takes into account the non-linearity of the PFD-charge-pump. The simulation is performed in discrete time on the prescaler and PFD-charge-pump circuit in open loop, which produces the input current pulses to the loop filter. The number of RF pulses at the output of the divider is counted, and compared to the PLL reference. This results in a phase error, which is converted to a charge pump current pulses. The resulting current pulses are injected in closed loop to render the output spectrum. Gain mismatch and dead-zone non-linearites can be modeled using this method. The simulation time is approximately 1 minute.

Fig. 3 and Fig. 4 show simulation results for a 3th order MASH converter and a PFD dead-zone of 1% and a gain mismatch of 5%. The reference frequency is 26 MHz and the fractional division number is 67.92 (16 bit accuracy). The output frequency is 1.76592 GHz, i.e 2.08 MHz from an integer multiple of the reference frequency. Spurious tones are visible in the output spectrum of the PFD (Fig. 3) as well as a noise floor of -80 dBc, although the $\Delta\Sigma$ output is perfectly randomized and dithered. Due to non-linearities in the PFD-charge-pump, noise folds back to lower offset frequencies and spurious tones reappear in the output spectrum. Fig. 4 shows the $\Delta\Sigma$ PSD for an ideal PFD and a non-linear PFD as it appears at the PLL output. As can be seen, due to non-linearities the output spectrum of the integer-N PLL (the dashed line) is seriously deteriorated by $\Delta\Sigma$ noise at lower offset frequencies.

4. Experimental results

4.1. The measurement setup

The $\Delta\Sigma$ fractional measurements are performed by controlling the PLL divider moduli with a HP80000 data generator, which generates the 4-bit control word (see Fig. 5). The 4-bit $\Delta\Sigma$ output bitstream is generated using MATLAB [7]. This provides a flexible way to test different kinds of $\Delta\Sigma$ modulator topologies and dithering patterns, without the need for redesigns.

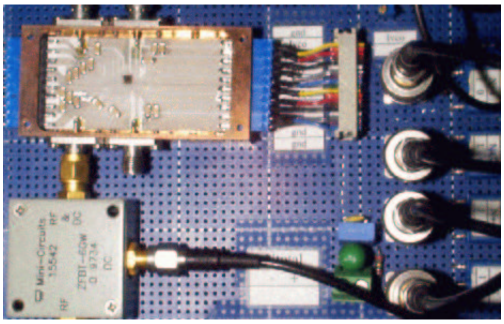

Figure 5. Photograph of the measurement setup

The influence of a 3-th order MASH modulator and of a 3-th order multi-bit, single loop modulator on the performance of the PLL is examined. $\Delta\Sigma$ MASH modulators are popular in fractional-N synthesis due to their ease of implementation in CMOS and unconditional stability. However, the MASH modulator employs a large range of moduli to synthesize a certain frequency, meaning that the prescaler has to switch over large ranges. A multi-bit single-loop modulator uses only a few moduli, reducing prescaler switching effects [8]. To ensure stability over the whole PLL modulus range, the output of the multi-bit modulator is a 5-bit word of which only the 4 MSBs are used.

Dithering sequences to further randomize the modulator outputs are applied to the modulators. To overcome the generation of a noise floor, the dithering sequences are noise shaped. Dithering at the input of the modulator must be third order shaped for a third order modulator.

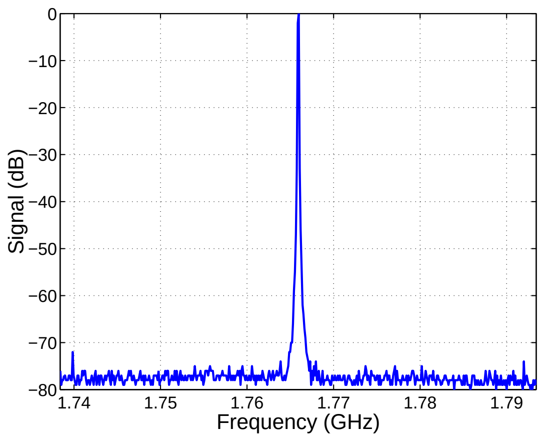

Figure 6. Measurement of the fractional-N PLL output spectrum

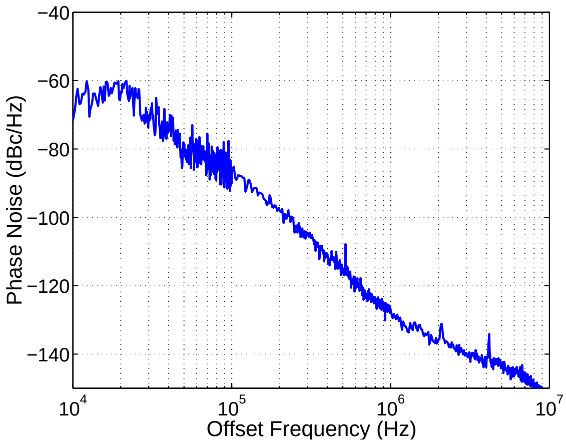

Figure 7. Phase Noise measurement with ΔΣ MASH converter at 1.76592 GHz

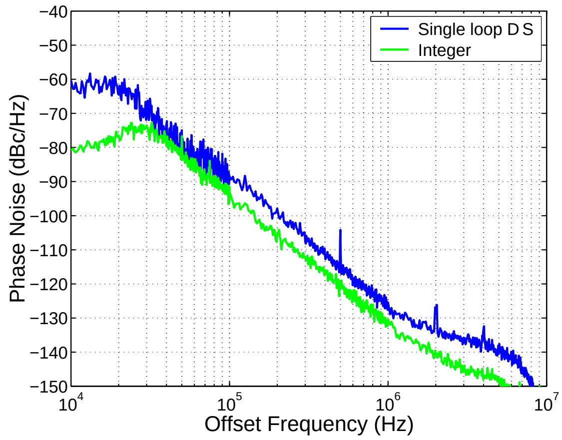

Figure 8. Phase noise measurement with multibit, single loop, ΔΣ converter at 1.76592 GHz (dark) and at integer frequency 1.768 GHz (light)

4.2. The measurement results

All measurements are performed with a 26 MHz reference frequency and at 1.76592 GHz, i.e. for a fractional division by 67.92. The input to the ΔΣ modulators is a 16-bit word (m=16), resulting in a frequency resolution of around 400 Hz. The unit charge pump current is set to 2 μA. The power supply voltage is only 2 V. Fig. 6 shows the output spectrum of the fractional-N PLL over a span of 55 MHz. The reference spurs are below -75 dBc, due to the careful charge pump design.

The measured phase noise of the PLL with a MASH modulator is presented in Fig. 7. Small spurs are present at 2 MHz as predicted by the simulations in Fig. 4. The spur level is well below -100 dBc, due to careful PFD-charge-pump design. The phase noise at 600 kHz is lower than -120 dBc/Hz. In Fig. 8 the measured phase of the PLL with a multi-bit, single loop modulator (dark) and at integer division (light) is compared. Noise at lower offsets originates from the ΔΣ modulator due to noise folding in the PFD, as predicted by the simulations. As a result, the RMS phase error $\Delta\Phi_{RMS}$ is increased from 1.7^o to 3^o. Note that the phase noise of the PLL at integer divisions is as low as -124 dBc/Hz at 600 kHz. The noisy measurements at low offsets and the increased noise floor can be proven to originate from noise coupling of the data generator.

The measured settling time of the PLL is 226 μs for a 100 MHz frequency step. The power consumption of the PLL is 70 mW from a 2 V power supply. The fully integrated, low-phase-noise VCO is responsible for almost 70% of the total power consumption. The IC area is 2x2 mm2, including bonding pads and bypass capacitors.

5. Conclusion

A 1.8 GHz 0.25 μm CMOS ΔΣ fractional-N frequency synthesizer, with integrated LC-VCO and loop filter is presented. The zero-dead zone phase detector is optimized towards linearity and spurious suppression.

Table 1. ΔΣ fractional-N PLL specification summary

Settling	226 μs
PN @ 600 kHz	< -120 dBc/Hz
$\Delta\Phi_{RMS}$	3^o
Reference Spurs	< -75 dBc
Fractional Spurs	< -100 dBc
Power	70 mW

Noise folding and fractional spur generation due to PFD non-linearities is simulated and experimentally verified. The measured phase noise is lower than -120 dBc/Hz at 600 kHz. Reference spurs are below -75 dBc, while the fractional spur level is lower than -100 dBc, due to the optimized PFD design.

6. Bibliography

[1] M. C. T. Riley and T. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 553–559, May 1993.

[2] J. Yuan and C. Svensson, "New single-clock CMOS latches and flip-flops with improved speed and power savings," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 62–69, Jan. 1997.

[3] J. Craninckx and M. Steyaert, *Low-Phase-Noise Fully Integrated CMOS Frequency Synthesizers*. Ph.D. Thesis, K.U. Leuven, 1997.

[4] B. De Muer, M. Borremans, N. Itoh, and M. Steyaert, "A 1.8 GHz highly-tunable, low-phase-noise CMOS VCO," in *Proceedings Custom Integrated Circuits Conference*, (Orlando), pp. 585–588, May 2000.

[5] F. Gardner, *Phaselock Techniques*. J. Wiley & Sons, New York, USA, 1979.

[6] B. Goldberg, *Digital techniques in frequency synthesis*. McGraw-Hill, 1995.

[7] T. M. Inc, *Matlab user's guide, version 5*. Prentice Hall, 1997.

[8] W. Rhee, B.-S. Song, and A. Ali, "A 1.1-GHz CMOS Fractional-N Frequency Synthesizer with a 3-b Third-Order ΔΣ Modulator ," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1453–1460, Oct. 2000.