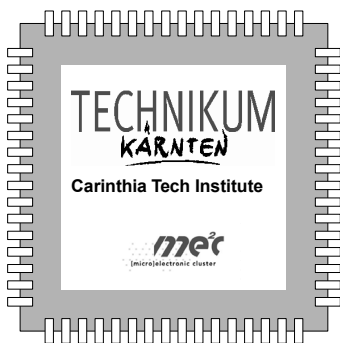


ESSCIRC 2001

**27th European
Solid-State Circuits Conference**

**18 – 20 September 2001
Villach, Austria**

Organised by:



and with

Technical Co-Sponsorship of the
IEEE Solid-State Circuits Society



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ESSCIRC ON INTERNET

<http://www.esscirc.org>

FOREWORD

Dear colleagues,

we cordially invite you to ESSCIRC 2001 which will be held in Villach, Austria, from 18 – 20 September 2001.

Villach - a charming old town with Mediterranean flair, surrounded by a vacation area with clear bathing lakes, traditional thermal baths and numerous summer and winter sport resorts - is the ideal backdrop for a successful conference.

But Villach is also home of world class high technology companies like Infineon and SEZ, research centres like Carinthia Tech Research and quality educational institutions like the Carinthia Tech Institute.

This year's conference is focused on Systems on Chip, RF/IF circuits, analogue and mixed signal circuits, optical circuits, power circuits and digital systems.

Invited papers will be given in the fields of Systems on Chip, foundry services for mixed signal systems, home entertainment systems, wireless systems, automotive busses, scaling and MEMs.

The technical programme of ESSCIRC 2001 includes 8 invited papers, 98 oral presentations and 31 posters, which have been carefully selected by renowned experts out of 196 submitted contributions from all over the world.

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In addition we offer a workshop on Systems on Chip on Monday and a Tutorial on Electronics in Automotive on Friday.

Furthermore there will be the possibility to visit the fab and design centre of Infineon on Monday afternoon and Friday morning.

Besides an interesting technical programme we will organise attractive evening events to show you a little bit from Villach and its beautiful surrounding and to offer the opportunity for informal talks in a relaxed atmosphere. For participants arriving the weekend before we offer an excursion to Venice and a scenic tour in Carinthia.

We look forward to welcoming you to Carinthia in September and hope that you will enjoy your stay in Villach.

Herbert Grünbacher
Reinhard Petschacher
Conference Chairmen

Franz Dielacher
Wolfgang Pribyl
TPC Chairmen

GENERAL INFORMATION

Carinthia

Carinthia is the southernmost province of Austria. It extends 9,533 km² to the south of the main alpine ridge and borders on Slovenia and Italy. 56% of the state lies above an altitude of 1,000 m, the climate is characterised by the Mediterranean influence.

For a good 2,000 years, the most direct route from the north to the south of Europe has led through the present-day Carinthia. Where the Roman legions once marched, the Tauern motorway today connects Hamburg with Palermo. It takes 3 hours from Munich to Villach and not much longer to the important Mediterranean ports of Trieste and Genova or the capital of Austria, Vienna.

Climate

Carinthia has a continental climate with Mediterranean influence. In September the average temperature is around 20°C during the day. During night it might be chilly (around 7°C).

Conference Venue

The Congress Center Villach is a multifunctional centre for a variety of scientific, economical, cultural and social events.

The architectural design of the building along the riverside is realised by a glass front, that offers a fantastic panoramic view overlooking the river Drau, the old town of Villach and the Karawanken mountains. This attractive design gives an airy and friendly atmosphere to the whole building.

Congress Center Villach
Europaplatz 1
A-9500 Villach
Tel: +43 4242 205-5804

Registration and Information Desk

The registration and information desk at the Congress Center Villach, will be open during the Congress as follows:

Monday	17 Sept.	08:00 – 21:00
Tuesday	18 Sept.	08:00 – 18:00
Wednesday	19 Sept.	08:00 – 18:00
Thursday	20 Sept.	08:00 – 16:00
Friday	21 Sept.	08:00 – 12:30

TRAVELLING TO VILLACH

How to reach Villach

Villach, Austria's gateway to the south, to both Italy and Slovenia, is a major road and railway junction at which the international lines between Vienna and Venice and between Munich and Ljubljana intersect.

By air

Klagenfurt airport is situated approximately 40 km from Villach. Regular flights from Frankfurt, Zurich and Vienna are operating daily. For detailed flight information visit the Klagenfurt Airport home page.

(<http://www.klagenfurt-airport.at/english>)

Shuttle Service

The Organising Committee offers a free-of-charge bus shuttle on Monday and Tuesday from Klagenfurt airport to Villach.

6 A questionnaire asking for your flight details will be mailed together with the confirmation of registration. Please make sure to return this questionnaire until **10 September 2001 at the latest**. If the Congress Secretariat does not receive your flight details concerning your arrival to Klagenfurt in time free shuttle transfer to Villach cannot be guaranteed.

On Thursday, 20 September a bus shuttle will be offered after the end of the morning session at 12:45 and after the closing session at 16:00. On Friday, 21 September a bus shuttle will be offered after the Tutorial at 13:45.

By train

Villach is a railway junction and hence easy to reach by train from Munich/Salzburg, Vienna, Venice and Ljubljana.

By road

Villach can be reached from Germany via the Felbertauern Tunnel or the Tauern Motorway (A10), from Switzerland via Innsbruck and the Felbertauern Tunnel, from Vienna via the Southern Motorway (A2), from Italy via Tarvisio (A2), and from Slovenia via the Karawanken Motorway (A11).

REGISTRATION

Every participant must register with the ESSCIRC 2001 Conference Secretariat. This applies to participants, speakers, and presenters. Participants are encouraged to pre-register for the congress to take advantage of lower fees and to ensure that their hotel accommodation requirements are met.

A registration form is included in the middle of this brochure. Alternatively registration is also possible via Internet at

<http://www.esscirc.org/esscirc2001/registration.htm>

Conference Registration Fees

	early until 10 August	late after
Full delegate	€ 410	€ 470
Student delegate	€ 200	€ 230
Accompanying person	€ 150	€ 150

Full registration fee includes attendance to the conference (Tuesday through Thursday), lunches and coffee breaks, Welcome Cocktail, Opening Dinner and Conference Banquet as well as the Conference Proceedings and CD-ROM.

Student registration fee (only B.Sc. and M.Sc. students are eligible, a proof of the university enrolment is required) includes attendance to the conference (Tuesday through Thursday), lunches and coffee breaks, the Welcome Cocktail as well as the CD-ROM. It is possible to register for the Opening Dinner and the Conference Banquet separately.

The **fee for accompanying persons** includes Welcome Cocktail, Opening Dinner and Conference Banquet as well as a city walk on Tuesday, 10.00 a.m.

Workshop Registration Fees

(additional to conference registration)

Monday, 17 Sept. - 08:45 – 17:00

Workshop – Systems on Chip, Systems in Package € 200
(including coffee breaks and lunch)

Friday, 21 Sept. - 08:30 – 12:30

Tutorial – Electronics in Automotive € 100
(including coffee break and lunch)

PAYMENT

All payments must be made in EURO and should be received before the Conference. Payments by bank transfer or by credit card (Visa and Mastercard are accepted). Please indicate the method of payment on the registration form.

- **Payment by credit card (VISA or Mastercard):**
Please indicate the credit card company, credit card number, name of cardholder, expiration date and the amount due on the registration form and do not forget to add your signature in the appropriate column.
- **Payment by bank transfer**
Please transfer directly to ESSCIRC 2001:
Bank: Creditanstalt Villach
 Hans-Gasser-Platz 5
 A-9500 Villach
Account number: 01814432900
Sort Code: 11810
SWIFT: CABVATWW

All bank charges must be prepaid and bank transfers must be clearly identified with the name of the participant and ESSCIRC 2001.

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CANCELLATION AND REFUND POLICY – REGISTRATION FEES

Before 10 August 2001	€ 50 handling fee
10 – 31 August 2001	50 % refund
After 31 August 2001	No refund

Refunds will be issued after the congress. Requests for a refund must be made in writing to the ESSCIRC 2001 Conference Secretariat.

LIABILITY AND INSURANCE

The organiser is not liable for personal injury and/or property damage resulting from burglary, theft, malicious damage, intentional and negligent property damage, and Acts of God during arrival, congress and departure. Every participant is liable for damage/injury whatever the reason may be, which he causes regardless if the damage/injury is caused by him/her or by the person accompanying him/her.

ACCOMMODATION

The Organising Committee reserved a sufficient number of rooms in hotels of different categories. Most of the hotels are located in the city centre within walking distance to the Congress Center Villach. Some of the hotels are situated in Warmbad Villach which is a spa area about 10 minutes by car from the city centre and in Velden situated on Lake Wörthersee about 20 minutes by car. A shuttle bus from Warmbad Villach and Velden to the Congress Centre will be available.

Hotel reservation will be made by the ESSCIRC 2001 Conference Secretariat. Please fill in the appropriate section on the registration form and indicate your hotel category preference (room rates are mentioned on the registration form). Early registration is highly recommended.

Please, give your credit card number (Visa or Mastercard) as guarantee for your hotel reservation. We will not deduct the amount due from your credit, only in case of cancellation we are legally entitled to debit your credit card according to the cancellation fees mentioned below.

CANCELLATION AND REFUND POLICY - HOTEL RESERVATIONS

Booking of accommodation is binding.

Before 31 August 2001	no charges
After 31 August 2001	the amount for one night will be charged to your credit card

Furthermore, the hotel is legally entitled to charge the customer for the stay booked at the hotel in case of cancellation after 15 September 2001 respectively in case of no-show.

Cancellations have to be made in writing (fax or e-mail) to the Congress Secretariat.

CHANGES AND MODIFICATIONS

Modifications of hotel bookings have to be made in writing (fax or e-mail) to the Congress Secretariat.

Short-termed reduction of the reservation period within seven days prior to arrival of the customer could occur the debit of a no-show charge in the amount of the room nights reduced.

EVENING PROGRAMME

Monday, 17 September 2001 – 19:00 – 21:00

Welcome Reception at the Congress Center Villach

(For all registered participants and accompanying persons)

Tuesday, 18 September 2001 – 19:30

Opening Dinner at the former Parkhotel

The *Parkhotel* was the leading hotel in Carinthia dating back to the Austrian-Hungarian monarchy and centre of the social life in Carinthia.

(For all registered delegates - full fee - and accompanying persons)

Wednesday, 19 September 2001 – 20:00

Conference Banquet

The Conference Banquet will take place in the Casino in Velden, a fashionable summer resort situated on Lake Wörthersee. For the banquet speech please see schedule. After the banquet you will have the opportunity to challenge your luck in the casino. To get started you get your first chip for free.

Bus departure: 18:30 from the Congress Center

(For all registered delegates - full fee - and accompanying persons)

10 EXCURSIONS – SUNDAY, 16 SEPT. 2001

(A minimum of 15 persons per excursion is required)

Scenic Tour Carinthia – 08:30 – 18:00

Drive along the south shore of Lake Wörthersee to the pilgrimage church of Maria Saal. Continuation to one of the most impressive castles in Austria, Hochosterwitz Castle. Lunch. Visit of the city of St. Veit an der Glan, the seat of the Dukes of Carinthia until 1518. Return along the scenic lake of Ossiach to Villach

Venice – 07:00 – 21:00

Charles Dickens once said “nothing in the world that you ever heard of Venice, is equal to the magnificent and stupendous reality“. Still, millions flock the city every year and remain, invariably, thrilled by their first impression of the Grand Canal.

Walking tour through the picturesque city including St. Mark’s Square, the Palazzo dei Dogi and Rialto Bridge. Lunch. Afternoon at leisure.

VISIT OF FAB AND DESIGN CENTRE OF INFINEON

Monday, 17 September

Bus departure: 15:00

Friday, 21 September

Bus departure: 09:00

Limited number of participants, registration required.

TECHNICAL PROGRAMME - GENERAL

Workshop

Monday, 17 September 2001

Workshop "Systems on Chip, Systems in Package"

Organiser: H. Tenhunen, KTH, Sweden

Tutorial

Friday, 21 September 2001

Tutorial "Electronics in Automotive"

Organiser: H. Zitta, Infineon, Austria

Conference

Invited: 8 speakers have been invited

Regular: 98 oral presentations

Posters: 31 poster presentations

The Poster Session is scheduled on Wednesday afternoon from 16:00 – 18:00. During this time authors will be present to answer questions. The posters will be displayed throughout the three conference days.

Awards

Best Paper Award 2000

The Best Paper Award 2000 will be presented by the last year's Technical Programme Chairman Kari Halonen, HUT, Finland, at the opening of this year's conference.

Best Paper Award 2001

The participants will be invited to select the Best Paper from the contributed papers presented this year. The Award will be presented at ESSCIRC 2002.

Best Poster Award 2001

The Best Poster Award 2001 will be presented during the closing session of the conference.

Conference Proceedings

Each registered participant (full registration) will receive a copy of the conference proceedings. Additional copies may be purchased during the conference. After the conference, please contact:

Editions Frontières / Seguir.Atlantica
Isabelle Delattre
3, Rue Seguir, F-75006 Paris, France
Tel: +33 1 55 42 61 40
Fax: +33 1 55 42 61 41
E-Mail: frontier@club-internet.fr

MON, 17.09.01 G.-V.-EINEM-SAAL 1

Workshop **Systems on Chip, Systems in Package**

Organiser: H. Tenhunen, KTH, Sweden

08:00 Registration

08:45 - 09:15 Introduction

H. Tenhunen
KTH, Stockholm, Sweden

09:15 - 12:30 Networks on Chip

A. Jantsch, J.-P. Soininen, M. Forsell, S. Kumar,
M. Millberg, J. Öberg
Royal Institute of Technology, Stockholm, Sweden
VTT Electronics, Oulu, Finland

As the number of processor cores and IP blocks integrated in a single chip is steadily growing, simple bus architectures will become infeasible. Within five to eight years we will be able to integrate an array of 32x32 processor cores on one integrated circuit. Current bus based architectures do not scale well to this size and synchronous domains will be confined to single cores with the consequence of having at least 1000 clock domains and global asynchronous communication on the chip.

In this presentation we investigate switch-based networks-on-chip and discuss the relevant problems spanning from physical issues to methodology.

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12:30 – 13:30 Lunch Break

13:30 - 17:00 Afternoon Session

Intrinsic compute efficiency, grain size, reconfigurable HW

J. Huisken
Philips, Eindhoven, The Netherlands

The different ways digital designs are made and will be made will be addressed: starting from the "intrinsic compute efficiency" (Claasen ISSCC'99) the differences in performance/area/power of CPUs/ DSPs/.../ASICs will be explained. In this context the place of re-configurable logic is, and why it is interesting will be analysed.

RF System On Chip: Interface Problems

M. Steyaert
KUL, Belgium

The integration of RF circuits is coming to a stage where attempts are made to integrate single chip RF systems, such as GSM, bluetooth and LAN devices. On top they try to integrate the RF front-end in standard CMOS technologies. Some pitfalls in integrating RF circuits and interference problems are addressed and discussed. The coupling mechanism of different building blocks to the sensitive RF circuits are addressed. Design cases of single chip RF transceivers are presented.

FRI, 21.09.01 G.-V.-EINEM-SAAL 1

Tutorial Electronics in Automotive

Organiser: H. Zitta, Infineon, Austria

08:00 Registration

08:30 Welcome and Introduction

H. Zitta, Infineon, Austria

08:45 - 12:30 Sessions

Smart Power Semiconductors for Innovative Automotive Solutions

C. Preuschoff, Infineon Technologies

Dedicated power semiconductor technologies are the enablers for new innovative solutions in automotive electronics. Key elements for this solutions in the Body, Safety and Powertrain area are: Reuse in circuit design, Smart Partitioning, High Integration and Advanced Backend Technologies.

Future Automotive Communication Architectures

St. Poledna,

TTTech Computertechnik AG, Austria

The digital revolution is conquering the automotive industry. A majority of present and future car features will be determined by electronics and software. Stand-alone control applications merge into integrated vehicle control systems. Furthermore x-by-wire technology is introduced from aerospace industry. This paradigm change imposes a demanding challenge to industry and on future automotive communication architectures.

The requirements for next generation vehicle bus systems demand highest level of safety and at the same time the convergence of all in vehicle communication including multimedia. Further requirements address the design process and development process. At the same time complexity grows, cost must be reduced to compete in the market.

Current trends clearly show that only time-triggered communication systems can provide the necessary control and precision needed. Based on experience from automotive x-by-wire projects this presentation will point out the wide range of tasks ahead and available solutions to this challenge.

Innovative SOI Technology for 12V / 42V Powernet

C. Mochel, Atmel Wireless & Microcontrollers

Recently, a new SOI technology was developed for the use in automotive applications. The lecture describes a high voltage, high power, high temperature SOI technology, the electrical and thermal properties and the benefits using this technology in automotive applications in comparison to bulk technologies.

12:30 – 13:30 Lunch Break

INVITED PAPERS

SoC Design from a Mixed Signal Perspective

Willy Sansen

Katholieke Universiteit Leuven, Belgium

(Tuesday, 18 September 2001, 09:20)

Mixed Signal Service and Foundry - A Business Model for the Future?

Wolfgang Pribyl

Austria Mikro Systeme, Unterpremstätten, Austria

(Tuesday, 18 September 2001, 10:00)

The potential of MEMS components for re-configurable RF interfaces in mobile communication terminals

Andreas Kaiser

IEMN - ISEN, Lille, France

(Tuesday, 18 September 2001, 14:00)

Microelectronics for Home Entertainment

Yoshiaki Hagiwara

Sony Corporation, Tokyo, Japan

(Wednesday, 19 September 2001, 08:30)

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Trends and Challenges in VLSI Technology Scaling Towards 100nm

Stefan Rusu

Intel Corporation, Santa Clara, CA, United States

(Wednesday, 19 September 2001, 14:00)

Integrated Circuits for Next Generation Wireless System

Josef Hausner

Infineon Technologies AG, Munich, Germany

(Thursday, 20 September 2001, 08:30)

Automated Processor Generation for System-on-Chip

Chris Rowen, Dror Maydan

Tensilica Inc., Santa Clara, CA, United States

(Thursday, 20 September 2001, 10:40)

Communication Bus for Automotive Applications

Stefan Poledna, Wolfgang Ettlmayr, Markus Novak

TTTech Computertechnik AG, Vienna, Austria

(Thursday, 20 September 2001, 14:00)

TUE, 18.09.01 JOSEF-RESCH-SAAL

09:00 to 09:20 Opening

09:20 Invited Paper

SoC Design from a Mixed Signal Perspective

W. Sansen

Katholieke Universiteit Leuven, Belgium

10:00 Invited Paper

Mixed Signal Service and Foundry - A Business Model for the Future?

W. Pribyl

Austria Mikro Systeme, Unterpremstätten, Austria

10:40 to 11:10 Coffee Break

Session 1.1: Synthesizers

Chairman: Q. Huang

ETH Zurich, Switzerland

11:10 A 17 mW, 2.5 GHz Fractional-N Frequency Synthesizer for CDMA-2000

S.-O. Lee¹, M. Yoh², J. Lee², I. Ryu²

¹Samsung Electronics, Seoul, Korea (South)

²Samsung Electronics, Korea (South)

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11:30 A 1.8 GHz CMOS Delta-Sigma Fractional-N Synthesizer

B. De Muer, M. Steyaert

Katholieke Universiteit Leuven, Belgium

11:50 An Injection Locking Scheme for Precision Quadrature Generation

R. Melville¹, D. Long¹, V. Gopinathan², P. Kinget³

¹Agere Systems, Murray Hill, NJ, United States

²Broadcom, Irvine, CA, United States

³Celight, Iselin, NJ, United States

12:10 A Wide-band, Compact, Fully Differential & Highly Accurate Integrated Phase Quadrature Locked Loop on 0.18 μm CMOS

S. Dedieu, F. Paillardet, I. Telliez

STMicroelectronics, Crolles, France

12:30 to 14:00 Lunch Break

TUE, 18.09.01 JOSEF-RESCH-SAAL

14:00 Invited Paper

The potential of MEMS components for re-configurable RF interfaces in mobile communication terminals

A. Kaiser

IEMN - ISEN, Lille, France

Session 1.2: Modulators / Demodulators

Chairman: D. Belot

STMicroelectronics, Crolles, France

14:40 A 14mA 2GHz 0.25 μ m CMOS Quadrature Demodulator Including a Low Phase Noise Local Oscillator

D. Pfaff, J. Rogin, Q. Huang

ETH Zurich, Switzerland

15:00 An Image-Reject Downconverter with Sideband Selection for Double-Conversion Receiver

K. Stadius¹, P. Paatsila², P. Järviö¹, K. Halonen¹

¹Helsinki University of Technology, Espoo, Finland

²Atmel Finland Development Center

15:20 A direct-conversion BiCMOS mixer

E. Tiiliharju, K. Halonen

Helsinki University of Technology, Espoo, Finland

15:40 1/f-Noise in Passive CMOS Mixers for Low and Zero IF Integrated Receivers

D. Leenaerts¹, W. Redman-White²

¹Philips Research Laboratories, Eindhoven, The Netherlands

²Philips Semiconductors and Southampton University, United Kingdom

16:00 to 16:30 Coffee Break

TUE, 18.09.01 JOSEF-RESCH-SAAL

Session 1.3: RF/IF Amplifiers

Chairman: W. Simbürger
Infineon Technologies AG, Munich, Germany

16:30 Improved High Dynamic Range Switched Gain Low-Noise Amplifier for Wide-Band CDMA Applications

P. Garcia, D. Belot
STMicroelectronics, Crolles, France

16:50 A 7-GHz 1.8dB NF CMOS Low Noise Amplifier

R. Fujimoto¹, K. Kojima², S. Otaka¹
¹Toshiba Corporation, Kawasaki, Japan
²Toshiba Semiconductors, Kawasaki, Japan

17:10 Variable Gain Amplifier for Dual Mode WCDMA/GSM Receivers

M.A.I. Mostafa¹, S.H.K. Embabi¹, M. Elmala²
¹Texas Instruments, Inc., Richardson, United States
²Texas A&M University, United States

17:30 Class 1 Bluetooth Power Amplifier with 24 dBm Output Power and 48% PAE at 2.4 GHz in 0.25 μm CMOS

V. Vathulya¹, T. Sowlati¹, D. Leenaerts²
¹Philips Research, Briarcliff Manor, NY, United States
²Philips Research, Eindhoven, The Netherlands

19:30 Opening Dinner at the former Parkhotel

TUE, 18.09.01 G.-V.-EINEM-SAAL 1

Session 1.4: Voltage Regulators

Chairman: P.J. Mole
Elantec Semiconductor UK Ltd., Harlow,
United Kingdom

11:10 A CMOS Voltage Reference Based on Weighted Difference of Gate-Source Voltages between PMOS and NMOS Transistors for Low Dropout Regulators

K.-N. Leung, P. K.T. Mok
Hong Kong University of Science and Technology, China

11:30 A High-Precision Low-Drop Linear Regulator for Battery Charging Application

D. Bernardon, M. Muellauer
Infineon Technologies, Villach, Austria

11:50 A Synchronous, Step-down from 3.6V to 1.0V, 1MHz PWM CMOS DC/DC Converter

I. Furukawa, Y. Sugimoto
Chuo University, Tokyo, Japan

12:10 Power Efficient Charge Pump in Deep Submicron Standard CMOS Technology

R. Pelliconi, D. Lezzi, A. Baroni, M. Pasotti, P.L. Rolandi
STMicroelectronics, Agrate Brianza, Italy

12:30 to 14:00 Lunch Break

TUE, 18.09.01 G.-V.-EINEM-SAAL 1

Session 1.5: Analogue Techniques

Chairman: C. Enz
CSEM SA, Neuchatel, Switzerland

14:40 A 1-V 15 μ W High-Precision Temperature Switch

D. Schinkel¹, R.-P. de Boer¹, A.-J. Annema¹,
A.J.M. van Tuijl²
¹University of Twente, Enschede, The Netherlands
²Philips Research Laboratories, Eindhoven, The Netherlands

15:00 Design and Measurement of a High Speed 2.5 Gbits/sec Laser Drive

S. Vandeweghe¹, E. Arslan², Z. Barton³, J. Vanneuvillle¹
¹IMEC-KHBO, Oostende, Belgium
²SIPEX, Zaventem, Belgium
³VUT, Brno, Czech Republic

15:20 An Offset Compensated Baseband Receive Channel for IS-95

D. Gubbins, A. Cahalane, C. Beghein, J. Morrissey,
G. Antonesei
Analog Devices, Limerick, Ireland

15:40 Integrated Offset Trimming Technique

S. Laville¹, S. Pontarollo¹, C. Dufaza², D. Auvergne²
¹STMicroelectronics, Grenoble, France
²LIRMM, Montpellier, France

16:00 to 16:30 Coffee Break

TUE, 18.09.01 G.-V.-EINEM-SAAL 1

Session 1.6: CMOS Imager

Chairman: R. Koch
Infineon Technologies, Munich, Germany

16:30 A CMOS VLSI Pilot and Support Chip for a Liquid Crystal on Silicon 8x8 Optical Cross-Connect

A. Lelah¹, G. Martel¹, T. Pérez-Segovia¹, P. Geoffroy¹,
J.-P. Laval¹, P. Jayet¹, P. Senn¹, B. Vinouze², P. Gravey³,
N. Wolffer³, R. Lever³, A. Tan³
¹France Telecom, Meylan, France
²Highwave Optical Technologies
³ENST Bretagne, Lannion, France

16:50 A 1Kx1K High Dynamic Range CMOS Image Sensor with On-Chip Programmable Region of Interest Readout

O. Schrey, J. Huppertz, G. Filimonovic, A. Bußmann,
W. Brockherde, B.J. Hosticka
Fraunhofer IMS, Duisburg, Germany

17:10 A CMOS Log Image Sensor with on-chip FPN Compensation

Y. Ni, K. Matou
Institut National des Telecommunications, Evry, France

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17:30 1.2 V 0.18 μm CMOS Imager with Column-Level Oversampling

J. Fortier, N.G. Tarr, A. Swaminathan, C. Plett
Carleton University, Ottawa, Canada

19:30 Opening Dinner at the former Parkhotel

TUE, 18.09.01 G.-V.-EINEM-SAAL 2

Session 1.7: Wireline Systems on Chip

Chairman: L. Kiss
Alcatel SA, Antwerpen, Belgium

11:10 A Single Chip Configurable Network Processor with built in ADSL-modem in 0.18 μm CMOS

C. Verdonck, D. Vandenameele
Alcatel Bell Hardware Design Centre, Antwerp, Belgium

11:30 An ADSL-RT Full-Rate Analog Frontend IC with Integrated Line Driver

H. Weinberger, A. Wiesbauer, C. Fleischhacker,
J. Hauptmann, T. Ferianz, M. Staber, D. Sträußnigg, B. Seger
Infineon Technologies, Design Center Villach, Austria

11:50 A four channel Integrated Voice and ADSL Full-Rate Analog Front-end

P. Pessl, C. Schranz, A. Di Giandomenico, S. Walter
Infineon Technologies MDCA, Villach, Austria

12:30 to 14:00 Lunch Break

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Session 1.8: Systems on Chip

Chairman: S. Donnay
IMEC DESICS, Leuven, Belgium

14:40 A Low Jitter, Low Power, CMOS 1.25-3.125Gbps Transceiver

A. Younis, C. Boecker, K. Hossain, F. Abughazaleh, B. Das,
Y. Chen, M. Robinson, S. Irwin, B. Grung
RocketChips, a Xilinx Company, Minneapolis, MN,
United States

15:00 A 10mW 2-Channel Fully Integrated System-on-Chip for Eddy-Current Position Sensing

M. Oberle, R. Reutemann, J. Hertle, Q. Huang
ETH Zurich, Switzerland

15:20 A Single Chip H.32X Multimedia Communication Processor with CIF 30f/s MPEG4/H.26X Bi-directional Codec

N. Minegishi, N. Motoyama, M. Takagi, F. Ogawa,
K. Shibata, N. Goda, K. Akiyoshi, T. Kamemaru,
K.-I. Asano
Mitsubishi Electric Corporation, Kanagawa, Japan

16:00 to 16:30 Coffee Break

TUE, 18.09.01 G.-V.-EINEM-SAAL 2

Session 1.9: Digital Systems

Chairman: S. Rusu

Intel Corporation, Santa Clara, CA, United States

16:30 A 53-GOPS Programmable Vision Processor for Processing, Coding-Decoding and Synthesizing of Images

U. Ramacher¹, W. Raab¹, N. Brüls¹, U. Hachmann¹,
C. Sauer¹, A. Schackow¹, J. Gliese¹, J. Harnisch¹,
M. Richter¹, E. Sicheneder¹, R. Schüffny², U. Schulz³,
H. Feldkämper³, C. Lütkemeyer³, H. Süsse⁴, S. Altmann⁴

¹Infineon Technologies AG, Munich, Germany

²University of Technology Dresden, Germany

³University of Technology RWTH Aachen, Germany

⁴Fraunhofergesellschaft IIS-EAS, Dresden, Germany

16:50 A Low-Power Parallel Processor IC for Digital Video Cameras

A. Abbo, R. Kleihorst, L. Sevat, P. Wielage, R. van Veen,
M. Op de Beeck, A. van der Avoird

Philips Research Laboratories, Eindhoven, Netherlands

17:10 A Low Jitter Digital Timing Synchronizer for CAP-based VDSL System

Y. Song¹, K. Lee², B. Kim¹

¹KAIST, Taejon, Korea (South)

²Stelsys Telecom Inc., Korea (South)

17:30 High-Performance Low-Power Carry Select Adder using Dual Transition Skewed Logic

W. Jeong, K. Roy, C.-K. Koh

Purdue University, West Lafayette, IN, United States

17:50 An Efficient Data Transmission Interface for VLSI Systems using Code-Division Multiple Access Technique

B.-K. Tan, R. Yoshimura, T. Matsuoka, K. Taniguchi

Osaka University, Japan

19:30 Opening Dinner at the former Parkhotel

WED, 19.09.01 JOSEF-RESCH-SAAL

08:30 Invited Paper

Microelectronics for Home Entertainment

Y. Hagiwara

Sony Corporation, Tokyo, Japan

Session 2.1: Optical Circuits 1

Chairman: J. Trontelj

University of Ljubljana, Slovenia

09:10 Low-Noise Sampling System for Photo Current Detection with Monolithically Integrated Photo Diodes

S. Groiss, J. Sturm

Infineon Technologies MDCA, Villach, Austria

09:30 BiCMOS OEIC with Enhanced Sensitivity for DVD Systems

K. Kieschnick¹, H. Zimmermann¹, P. Seegebrecht²

¹Technische Universität Wien, Vienna, Austria

²Christian-Albrechts-Universität, Kiel, Germany

09:50 A Fully Integrated CMOS Light to Logic Fiber Optic Receiver Circuit

K. Schroedinger, J. Stimma, M. Mauthe

Infineon Technologies AG, Berlin, Germany

10:10 to 10:40 Coffee Break

WED, 19.09.01 JOSEF-RESCH-SAAL

Session 2.2: Optical Circuits 2

Chairman: W. Brockherde
Fraunhofer IMS, Duisburg, Germany

10:40 Bandwidth Enhancement Techniques for Transimpedance Amplifier in CMOS Technologies

C.-H. Lu, W.-Z. Chen
National Central University, Chung-Li, Taiwan

11:00 A 2.5Gb/s CMOS Transimpedance Amplifier Using Novel Active Inductor Load

Y.-H. Oh, S.-G. Lee, H.-H. Park
Information and Communication University, Daejeon, Korea (South)

11:20 Novel cell-AGC technique for Burst-Mode CMOS Preamplifier with Wide Dynamic Range and High Sensitivity for ATM-PON System

S. Yamashita¹, S. Ide¹, K. Mori¹, A. Hayakawa², N. Ueno³, K. Tanaka¹

¹Fujitsu Laboratories Ltd., Kanagawa, Japan

²Fujitsu VLSI Ltd., Japan

³Fujitsu Ltd., Japan

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11:40 SiGe BiCMOS Burst-Mode 155 Mb/s Receiver for PON

S. Brigati¹, P. Colombara², L. D'Ascoli², U. Gatti³, T. Kerekes⁴, P. Malcovati⁵, A. Profumo⁶

¹ACCO Microelectronica S.r.l., Pavia, Italy

²Infineon Technologies, Milan, Italy

³Siemens ICN S.p.A., Milan, Italy

⁴Austria Mikro Systeme Int. AG, Unterpremstätten, Austria

⁵University of Pavia, Italy

⁶Italtel S.p.A., Milan, Italy

12:00 A Low Noise, Wide Dynamic Range, Transimpedance Amplifier with Automatic Gain Control for SDH/SONET (STM16/OC48) in a 30GHz f_T BiCMOS Process

M.A.T. Sanduleanu¹, P. Manteman²

¹Philips Research Eindhoven, The Netherlands

²Philips Semiconductors Nijmegen, The Netherlands

12:20 to 14:00 Lunch Break

WED, 19.09.01 JOSEF-RESCH-SAAL

14:00 Invited Paper

Trends and Challenges in VLSI Technology Scaling Towards 100nm

S. Rusu

Intel Corporation, Santa Clara, CA, United States

Session 2.3: Optical Image Processing

Chairman: V. Kempe

AMS, Unterpemstatten, Austria

14:40 Analog Pattern Classifier with Flexible Matching Circuitry Based on Principal-Axis-Projection Vector Representation

T. Yamasaki, K. Yamamoto, T. Shibata

The University of Tokyo, Bunkyo-ku, Japan

15:00 ACE16K: an Advanced Focal-Plane Analog Programmable Array Processor

G. Linan, R. Dominguez-Castro, S. Espejo,

A. Rodriguez-Vazquez

Instituto de Microelectronica de Sevilla, Spain

15:20 A Current-Mode 64x1 Programmable Gabor Filter for Early Vision Systems

F. Borghetti¹, P. Malcovati¹, F. Maloberti²

¹University of Pavia, Italy

²Texas A&M University, College Station, TX, United States

15:40 A low-power CMOS silicon retina for feature extraction in real-time, embedded systems

M. Barbaro, L. Raffo

University of Cagliari, Italy

16:00 A General-Purpose CMOS Vision Chip with a Processor-Per-Pixel SIMD Array

P. Dudek, P.J. Hicks

UMIST, Manchester, United Kingdom

16:00 to 18:00 Poster Session (Foyer First Floor)

20:00 Conference Banquet

Banquet Address

What is Silicon Valley's Success Based on - Silicon or Entrepreneurship?

Shyam Kamath

Professor of Economics and Director of Executive Programs
California State University, Hayward

WED, 19.09.01 G.-V.-EINEM-SAAL 1

Session 2.4: Power Circuits

Chairman: G. Melcher

Infineon Technologies, Graz, Austria

09:10 A Robust Smart Power Bandgap Reference Circuit for Use in an Automotive Environment

W. Horn, H. Zitta

Infineon Technologies MDCA, Villach, Austria

09:30 Thermal Destruction Testing: an Indirect Approach to a Simple Dynamic Thermal Model of Smart Power Switches

M. Glavanovics, H. Zitta

Infineon Technologies MDCA, Villach, Austria

09:50 A 250 W Audio Amplifier with Straightforward Digital Input-PWM Output Conversion

A. Grosso¹, E. Botti¹, M. Ghioni², F. Stefani¹

¹STMicroelectronics, Cornaredo, Italy

²Politecnico di Milano, Italy

10:10 to 10:40 Coffee Break

WED, 19.09.01 G.-V.-EINEM-SAAL 1

Session 2.5: Mixed Signal Communciation Circuits

Chairman: P. Senn
France Telecom, Meylan, France

10:40 High-Speed CMOS Analog Viterbi Detector for 4-PAM Partial Response Signalling

B. Zand, D. Johns
University of Toronto, Canada

11:00 A 100Mb/s, 2.8V CMOS Current-Mode Analogue Viterbi Decoder

A. Demosthenous, J. Taylor
University College London, United Kingdom

11:20 A New Impedance Control Circuit for USB2.0 Transceiver

K.-H. Koo, J.-H. Seo, J.-W. Kim
SAMSUNG Electronics, Youngin-City, Korea (South)

11:40 Digitally tuneable on-chip line termination resistor for 2.5Gbit/s LVDS receiver in 0.25 μ m standard CMOS technology

M. Kumric, F. Ebert, R. Ramp, K. Welch
Alcatel SEL AG, Stuttgart, Germany

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12:00 A Fully Integrated Analog Frontend Macro for Cable Modem Applications in 0.18 μ m CMOS

A. Wiesbauer¹, M. Clara¹, M. Harteneck², T. Pötscher¹,
C. Fleischhacker¹, G. Koder¹, C. Sandner¹
¹Infineon Technologies MDCA, Villach, Austria
²Infineon Technologies DC, Munich, Germany

12:20 to 14:00 Lunch Break

WED, 19.09.01 G.-V.-EINEM-SAAL 1

Session 2.6: Mixed Signal Systems

Chairman: A. Kaiser
IEMN - ISEN, Lille, France

14:40 Smart Power Integrated Circuit for piezoceramic-based microrobot

E. Montané, S Bota, J. López-Sánchez, P. Miribel-Català,
M. Puig-Vidal, J. Samitier
Universitat de Barcelona, Spain

15:00 A 1 μ A Front-End for Pacemaker Atrial Sensing Channels

L. Lentola¹, A. Mozzi¹, A. Neviani², A. Baschirotto³
¹Medico S.p.A., Rubano, Italy
²University of Padova, Italy
³University of Lecce, Italy

15:20 NMOS-based Gaussian-Element-Matching Analog Associative Memory

M. Ogawa, T. Shibata
The University of Tokyo, Bunkyo-ku, Japan

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15:40 A Low Power Digital Beamformer for Handheld Ultrasound Systems

V.S. Gierenz, R. Schwann, T.G. Noll
University of Technology RWTH Aachen, Germany

16:00 Noise-Constrained Design of Reliable Power Networks for Mixed-Power Supply Systems

J. Lee¹, S. Kang²
¹University of Illinois, Urbana, IL, United States
²University of California, Santa Cruz, CA, United States

16:00 to 18:00 Poster Session (Foyer First Floor)

20:00 Conference Banquet

Banquet Address

What is Silicon Valley's Success Based on - Silicon or Entrepreneurship?

Shyam Kamath
Professor of Economics and Director of Executive Programs
California State University, Hayward

WED, 19.09.01 G.-V.-EINEM-SAAL 2

Session 2.7: Building Blocks for Digital Systems

Chairman: S. Rusu
Intel Corporation, Santa Clara, CA, United States

09:10 VLSI Implementation of a High Performance and Low Power 32-Bit Multiply-Accumulate Unit

Y. Liao, D. Roberts, E. Hoffman
Intel Corporation, Chandler, AZ, United States

09:30 A Direct Digital Frequency Synthesizer Using A New ROM Compression Method

B.-D. Yang¹, K.-H. Sung¹, Y.-J. Kim¹, L.-S. Kim¹,
S.-H. Han², H.-K. Yu²
¹KAIST, Taejon, Korea (South)
²ETRI, Taejon, Korea (South)

09:50 Design of a CORDIC-Based SIN/COS Intellectual Property (IP) Using Predictable Sign Bits

T.-P. Chuang, C.-C. Huang, S.-F. Hsiao
National Sun Yat-Sen University, Kaohsiung, Taiwan

10:10 to 10:40 Coffee Break

WED, 19.09.01 G.-V.-EINEM-SAAL 2

Session 2.8: Memory and Interface Circuits

Chairman: H. Veendrick
Philips Research Laboratories, Eindhoven,
The Netherlands

10:40 0.13um 32Mb/64Mb Embedded DRAM Core with High Efficient Redundancy and Enhanced Testability

H. Kikukawa¹, S. Tomishima², T. Tsuji², T. Kawasaki¹,
S. Sakamoto¹, M. Ishikawa², W. Abe¹, H. Tanizaki³,
H. Kato³, T. Uchikoba¹, T. Inokuchi¹, M. Senoh¹,
Y. Fukushima¹, M. Niuro³, M. Maruta³, A. Shibayama¹,
T. Ooishi³, K. Takahashi¹, H. Hidaka²

¹Matsushita Electric Industrial Co. Ltd., Kyoto, Japan

²Mitsubishi Electric Corp., Japan

³Mitsubishi Electric Engineering Co. Ltd., Japan

11:00 A Simple Low Voltage Current Sense Amplifier with Switchable Input Transistor

B. Wicht¹, D. Schmitt-Landsiedel¹, S. Paul²

¹Technical University of Munich, Germany

²Infineon Technologies AG, Munich, Germany

11:20 A 0.8V, 9ns, 0.77mW at 50MHz, 128Kb, Four-Way, Set-Associative, 2-Level CMOS Cache Memory

J.B. Kuo¹, P.-F. Lin²

¹University of Waterloo, Canada

²NTUEE

11:40 A High-Speed Memory Interface Circuit Tolerant to PVT Variations and Channel Noise

J.-Y. Park¹, Y. Koo¹, D.-K. Jeong¹, W. Kim¹, C. Yoo²,
C. Kim²

¹Seoul National University, Korea (South)

²Samsung Electronics Co., Kiheung, Korea (South)

12:00 Bus Data Encoding with Coupling-driven Adaptive Codebook Method for Low Power Data Transmission

S. Komatsu, M. Ikeda, K. Asada

University of Tokyo, Bunkyo, Japan

12:20 to 14:00 Lunch Break

WED, 19.09.01 G.-V.-EINEM-SAAL 2

Session 2.9: Digital Circuits Design Techniques

Chairman: A. Rothermel
Universität Ulm, Germany

14:40 Reduction of Interconnect Delay by Exploiting Cross-talk

S. van Dijk¹, D. Hély²

¹Philips Research Laboratories, Eindhoven, The Netherlands

²National Institute of Applied Sciences of Lyon, France

15:00 Speed and Behaviour Improvement for Semidynamic Flip-Flop Logic Family

M. Graziano, G. Masera, G. Piccinini, M. Zamboni
Politecnico di Torino, Italy

15:20 A Leakage Tolerant High Fan-in Dynamic Circuit Design Technique

J.-J. Kim, K. Roy

Purdue University, West Lafayette, IN, United States

15:40 Power Saving in CMOS Using a Half-Swing Clocking Scheme

M. Loew¹, H.-J. Pfleiderer¹, N. Bruels²

¹University of Ulm, Germany

²Infineon Technologies AG, Germany

16:00 MTCMOS Sequential Circuits

J. Kao, A. Chandrakasan

Massachusetts Institute of Technology, Cambridge, MA,
United States

16:00 to 18:00 Poster Session (Foyer First Floor)

20:00 Conference Banquet

Banquet Address

What is Silicon Valley's Success Based on - Silicon or Entrepreneurship?

Shyam Kamath

Professor of Economics and Director of Executive Programs
California State University, Hayward

WED, 19.09.01 FOYER FIRST FLOOR

16:00 to 18:00 Poster Session

A MEMS-based rotational accelerometer for HDD applications with 2.5rad/sec² resolution and digital output

A. Gola¹, N. Bagnalasta¹, P. Bendiscioli¹, E. Chiesa¹,
S. Delbo¹, E. Lasalandra¹, F. Pasolini¹, M. Tronconi¹,
T. Ungaretti¹, A. Baschiroto²

¹STMicroelectronics, Cornaredo, Italy

²University of Lecce, Italy

3.6 GHz VCOs for multi-band GSM transceivers

J. Kucera, B.-U. Klepser

Infineon Technologies, Munich, Germany

Integrated LC-tuned VCO in BiCMOS process

N. Itoh, S.-I. Ishizuka, K. Katoh

Toshiba Corporation, Kawasaki, Japan

Fast Frequency Acquisition Phase-Frequency Detectors for GSA/s Phase-Locked Loops

M. Mansuri¹, D. Liu², C.-K. Yang¹

¹University of California at Los Angeles, United States

²Stanford University, United States

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A 1.5V, 1.7mA 700 MHz CMOS LC Oscillator with No Upconverted Flicker Noise

K. Hoshino, E. Hegazi, J. Rael, A. Abidi

University of California, Los Angeles, CA, United States

A 2.4GHz Wide Tuning Range VCO with Automatic Level Control Circuitry

J. Rogers¹, D. Rahn¹, C. Plett²

¹SiGe Semiconductor, Ottawa, Canada

²Carleton University, Ottawa, Canada

A Wideband IMRR improving quadrature mixer/LO generator

P. Vancorenland, M. Steyaert

Katholieke Universiteit Leuven, Belgium

A Redundant-Cell-Relay Continuous Self-Calibration Method for Current-Steering DACs

W. Zhang, M. Hassoun

Iowa State University, Richardson, TX, United States

A Low Voltage Low Power High Performance Fully Integrated DTMF receiver

D. Vázquez¹, M.J. Avedillo², G. Huertas², J.M. Quintana²,
M. Pauritsch³, A. Rueda¹, J.L. Huertas¹

¹Universidad de Sevilla, Spain

²Universidad de Sevilla / IMSE-CNM, Spain

³Austria Mikro Systeme Int. AG, Unterpemstätten, Austria

WED, 19.09.01 FOYER FIRST FLOOR

A Pipelined Analog-to-Digital Converter for Low Temperatures

T. Mäkineniemi¹, P. Kosonen²

¹Nokia Networks, Espoo, Finland

²Nokia Research Center, Helsinki, Finland

Design of an integrated CMOS operational amplifier with low probability EMI induced failures

A. Richelli¹, L. Colalongo¹, M. Quarantelli²,

Z.M. Kovacs-Vajna¹

¹University of Brescia, Italy

²PDF Solutions, Italy

Simple Scalable CMOS Linear Regulator Architecture

R. Antheunis, I. van Loo

Philips Semiconductors, Nijmegen, The Netherlands

Low Swing Signaling Using a Dynamic Diode-Connected Driver

M. Ferretti, P.A. Beerel

University of Southern California, Los Angeles, CA,
United States

Analysis of the Floating Voltage Transfer Characteristic and Comparison of Circuit Styles in Partially Depleted SOI-CMOS

K.K. Das, R.B. Brown

University of Michigan, Ann Arbor, MI, United States

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An 8x8 Sub-Threshold Digital CMOS Carry Save Array Multiplier

B. Paul, H. Soeleman, K. Roy

Purdue University, West Lafayette, IN, United States

Evaluation of Skew Tolerance in Delayed Clocking Scheme for Dynamic Circuits

M. Garg, A. Katoch

Philips Research Laboratories, Eindhoven, The Netherlands

Configurable Area-IO Memory for System-in-a-Package (SiP)

M. Wang¹, K. Suzuki¹, W. Dai¹, A. Sakai², K. Watanabe³

¹University of California, Santa Cruz, CA, United States

²Sanyo Electric Co., Ltd., Japan

³Tokyo Institute of Technology, Japan

Code Memory Compression with Online Decompression

C. Piguet, P. Volet, J.-M. Masgonty, F. Rampogna,

P. Marchal

CSEM, Neuchâtel, Switzerland

A flexible Datapath Generator for Physical Oriented Design

O. Weiß, M. Gansen, T.G. Noll

University of Technology RWTH, Aachen, Germany

WED, 19.09.01 FOYER FIRST FLOOR

Built-In Self-Repair IC Logic with Area Optimized Error-Correcting Codes

R. Kleihorst, N. Benschop

Philips Research Laboratories, Eindhoven, The Netherlands

A 30 MHz DDS clock generator with 8-bit, 130 ps delay generator and -50 dBc spurious level

A. Heiskanen, A. Mäntyniemi, T. Rahkonen

University of Oulu, Finland

A True 1V CMOS Log-Domain Analog Hearing-Aid-on-a-Chip

F. Serra-Graells¹, L. Gómez², Ò. Farrés¹

¹Centro Nacional de Microelectrónica, Bellaterra, Spain

²Microson S.A., Barcelona, Spain

Analyzing heterogeneous system architectures by means of cost functions: A comparative study for basic operations

H. Blume, H. T. Feldkämper, H. Hübner, T. G. Noll

University of Technology RWTH, Aachen, Germany

A Microcontroller Embedded ASIC for an Implantable Electro-Neural Stimulator

C. Hitzelberger¹, Y. Manoli¹, R. Hakenes², S. Groß³

¹University of Saarland, Saarbrücken, Germany

²Micronas GMBH, Freiburg, Germany

³Netfab GMBH, Saarbrücken, Germany

A 2.4-GHz Single-Pole Double-Throw T/R Switch with 0.8-dB Insertion Loss Implemented in a CMOS Process

F.-J. Huang, K. O

University of Florida, Gainesville, FL, United States

Design and Analysis Methodology for a Bluetooth Sub-micron CMOS PA

V. Knopik¹, D. Gerna¹, D. Belot¹, M. Castagné²,

D. Gasquet², L. Nativel²

¹STMicroelectronics, Crolles, France

²University of Montpellier II, France

Performance study of CMOS power amplifiers

K. Mertens, P. Reynaert, M. Steyaert

Katholieke Universiteit Leuven, Belgium

A Low Voltage, Low Power RF CMOS LNA for Bluetooth Applications using Transmission Line Transformer

B. Toole, C. Plett

Carleton University, Ottawa, Canada

WED, 19.09.01 Foyer First Floor

Creating flexible analogue IP blocks

R. Castro-Lopez, F.V. Fernandez, F.V. Fernandez,
M. Delgado-Restituto, F. Medeiro, A. Rodriguez-Vazquez
IMSE-CNM, Sevilla, Spain

A Silicon Efficient High Speed $L = 3$ rate $1/2$ Convolutional Decoder Using Recurrent Neural Networks

A. Rantala, S. Vatunen, T. Harinen, M. Aberg
VTT Electronics, Finland

Creating flexible analogue IP blocks

R. Castro-Lopez, F.V. Fernandez, F.V. Fernandez,
M. Delgado-Restituto, F. Medeiro, A. Rodriguez-Vazquez
IMSE-CNM, Sevilla, Spain

IP-Reusable 32-Bit VLIW Risc Core

F. Campi¹, R. Guerrieri¹, R. Canegallo²

¹University of Bologna, Italy

²STMicroelectronics, Italy

THU, 20.09.01 JOSEF-RESCH-SAAL

08:30 Invited Paper

Integrated Circuits for Next Generation Wireless System

J. Hausner

Infineon Technologies AG, Munich, Germany

Session 3.1: Integrated Microsystems

Chairman: R. Hasholzner

Motorola Entertainment Solutions, Munich,
Germany

09:10 A Smart Wind Sensor using Time-Multiplexed Thermal Sigma-Delta Modulators

K. Makinwa, J. Huijsing

Delft University of Technology, The Netherlands

09:30 A Monolithic Positioning System

R. Wunderlich, C. Thomas, K. Schumacher

University of Dortmund, Dortmund, Germany

09:50 An Integrated CMOS Microsystem for NMR Applications

J. Frounchi, G. Boero, B. Furrer, P.-A. Besse, R.S. Popovic

Swiss Federal Institute of Technology (EPFL), Lausanne,
Switzerland

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10:10 to 10:40 Coffee Break

THU, 20.09.01 JOSEF-RESCH-SAAL

10:40 Invited Paper

Automated Processor Generation for System-on-Chip

C. Rowen, Dror Maydan

Tensilica Inc., Santa Clara, CA, United States

Session 3.2: IP-blocks for Telecommunications

Chairman: J. Nurmi

Tampere University of Technology, Finland

11:20 Low-Cost IP-blocks for UMTS turbo decoders

G. Masera, M. Mazza, G. Piccinini, F. Viglione, M. Zamboni

Politecnico di Torino, Italy

11:40 Scalable, Power and Area Efficient High Throughput Viterbi Decoder Implementations

T. Gemmeke, V.S. Gierenz, T.G. Noll

University of Technology RWTH, Aachen, Germany

12:00 Implementation of an efficient Lattice Digital Ladder Filter for up/down conversion in an OFDM-WLAN system

S. Signell¹, T. Fonden¹, M. Badaroglu², S. Donnay²

¹Ericsson Radio Systems, Stockholm, Sweden

²IMEC, Leuven, Belgium

12:20 to 14:00 Lunch Break

THU, 20.09.01 JOSEF-RESCH-SAAL

14:00 Invited Paper

Communication Bus for Automotive Applications

S. Poledna, W. Ettlmayr, M. Novak

TTTech Computertechnik AG, Vienna, Austria

Session 3.3: Transceiver Building Blocks

Chairman: K. Halonen

Helsinki University of Technology, Finland

14:40 Low-Power Complex Polynomial Predistorter Circuit in CMOS for RF Power Amplifier Linearization

E. Westesson¹, L. Sundström²

¹Lund University, Sweden

²Ericsson Mobile Communications AB, Lund, Sweden

15:00 A CMOS AGC-less IF Strip for Bluetooth

V. Prodanov, G. Palaskas, J. Glas, V. Bocuzzi

Agere Systems, Murray Hill, NJ, United States

15:20 GSM/DCS1800 Dual Band Direct-Conversion Transceiver IC with a DC Offset Calibration System

S. Tanaka¹, T. Yamawaki¹, K. Takikawa¹, N. Hayashi¹,

I. Ohno¹, T. Wakuta¹, S. Takahashi¹, M. Kasahara¹,

B. Henshaw²

¹Hitachi. Ltd, Japan

²TTP Communication Ltd.

15:40 to 16:00 Closing Session

THU, 20.09.01 G.-V.-EINEM-SAAL 1

Session 3.4: VCO Circuits

Chairman: H. Klar
Technische Universität Berlin, Germany

09:10 A CMOS 10 GHz Voltage Controlled LC-Oscillator with integrated high-Q inductor

W. De Cock, M. Steyaert
Katholieke Universiteit Leuven, Belgium

09:30 Comparison of CMOS VCOs for UMTS Tuned by Standard and Novel Varactors in Standard 0.25 μ m Technology

J. Maget¹, M. Tiebout¹, R. Kraus²
¹Infineon Technologies AG, Munich, Germany
²University of Bundeswehr, Neubiberg, Germany

09:50 1GHz Tuning Range, Low Phase Noise, LC Oscillator with Replica Biasing Common-Mode Control and Quadrature Outputs

M.A.T. Sanduleanu¹, J.P. Frambach²
¹Philips Research, Eindhoven, The Netherlands
²Philips Semiconductors, Nijmegen The Netherlands

10:10 to 10:40 Coffee Break

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Session 3.5: Oscillators and Synthesizers

Chairman: M. Steyaert
Katholieke Universiteit Leuven, Belgium

11:20 A Fully Integrated 2.4GHz LC-VCO Frequency Synthesizer with 3.5ps Jitter in 0.18 μ m Standard Digital CMOS Copper Technology

N. Da Dalt, S. Derksen, P. Greco, C. Sandner, H. Schmid,
K. Strohmayer
Infineon Technologies Austria, Villach, Austria

11:40 A Low Phasenoise, Differentially Tuned, 1.8GHz Power VCO with an ESD-compatible 14dBm Output Stage in Standard Digital CMOS

T. Liebermann, M. Tiebout
Infineon Technologies AG, Munich, Germany

12:00 1200 MHz fully integrated VCO with "turbo-charger" technique

N. Itoh, S.-I. Ishizuka
Toshiba Corporation, Kawasaki, Japan

12:20 to 14:00 Lunch Break

THU, 20.09.01 G.-V.-EINEM-SAAL 2

Session 3.7: Band Pass Sigma Delta

Chairman: F. Op't Eynde
Alcatel Microelectronics, Zaventem, Belgium

09:10 A Fourth-Order Bandpass Delta-Sigma Modulator Using Second-Order Bandpass Noise-Shaping Dynamic Element Matching

T. Ueno¹, A. Yasuda², T. Yamaji¹, T. Itakura¹

¹Toshiba Corporation, Kawasaki, Japan

²Texas Instruments Japan Limited

09:30 A 1.2V Direct Background Digital Tuned Continuous-Time Bandpass Sigma-Delta Modulator

H. Huang, E. Lee

Iowa State University, Ames, Iowa, United States

09:50 A 80MHz Band-Pass Delta-Sigma Modulator for a 100MHz IF-receiver

T. Salo¹, S. Lindfors², K. Halonen¹

¹Helsinki University of Technology, Espoo, Finland

²Royal Institute of Technology

40 10:10 to 10:40 Coffee Break

Session 3.8: Sigma Delta Converters

Chairman: A. Rodriguez-Vazquez
University of Sevilla, Spain

11:20 A 1-V, 10-MHz Clock-Rate, 13-bit CMOS Delta-Sigma Modulator Using Unity-Gain-Reset Opamps

M. Keskin, U.-K. Moon, G. Temes

Oregon State University, Corvallis, OR, United States

11:40 A 12-Bit Power Efficient Continuous-Time Sigma-Delta Modulator with 250 μ W Power Consumption

F. Gerfers, M. Ortmanns, Y. Manoli

University of Saarland, Saarbruecken, Germany

12:00 A 98dB 3.3V 28mW-per-channel multibit audio DAC in a standard 0.35 μ m CMOS technology

M. Annovazzi¹, V. Colonna¹, G. Gandolfi¹, A. Baschiroto²

¹STMicroelectronics, Cornaredo, Italy

²University of Lecce, Italy

12:20 to 14:00 Lunch Break

THU, 20.09.01 G.-V.-EINEM-SAAL 2

Session 3.9: Data Converters

Chairman: B. Nauta

University of Twente, Enschede, The Netherlands

14:40 A 3.2-mA 6-bit pipelined A/D converter for a Bluetooth^{TM1} RF transceiver

J. Kudoh¹, T. Matsuura¹, E. Imaizumi²

¹Hitachi Ltd., Gunma-ken, Japan

²Hitachi ULSI Systems Co.,Ltd, Tokyo, Japan

15:00 A GSM Receiver Base Band in 0.25 μ m, 1.8V Fully Depleted SOI Including a 4th Order Serial Sigma-Delta A/D Converter

E. Compagne¹, J. Sevenhans², C. Raynaud³

¹Dolphin Integration, Meylan, France

²Alcatel, Antwerpen, Belgium

³LETI-CEA, Grenoble, France

15:20 Histogram Based Correction of Matching Errors in Subranged ADC

J. Elbornsson¹, J.-E. Eklund²

¹Linköping University, Sweden

²Ericsson Microelectronics AB, Linköping, Sweden

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