

A Switched-Capacitor Variable Gain Amplifier for CCD Image Sensor Interface System

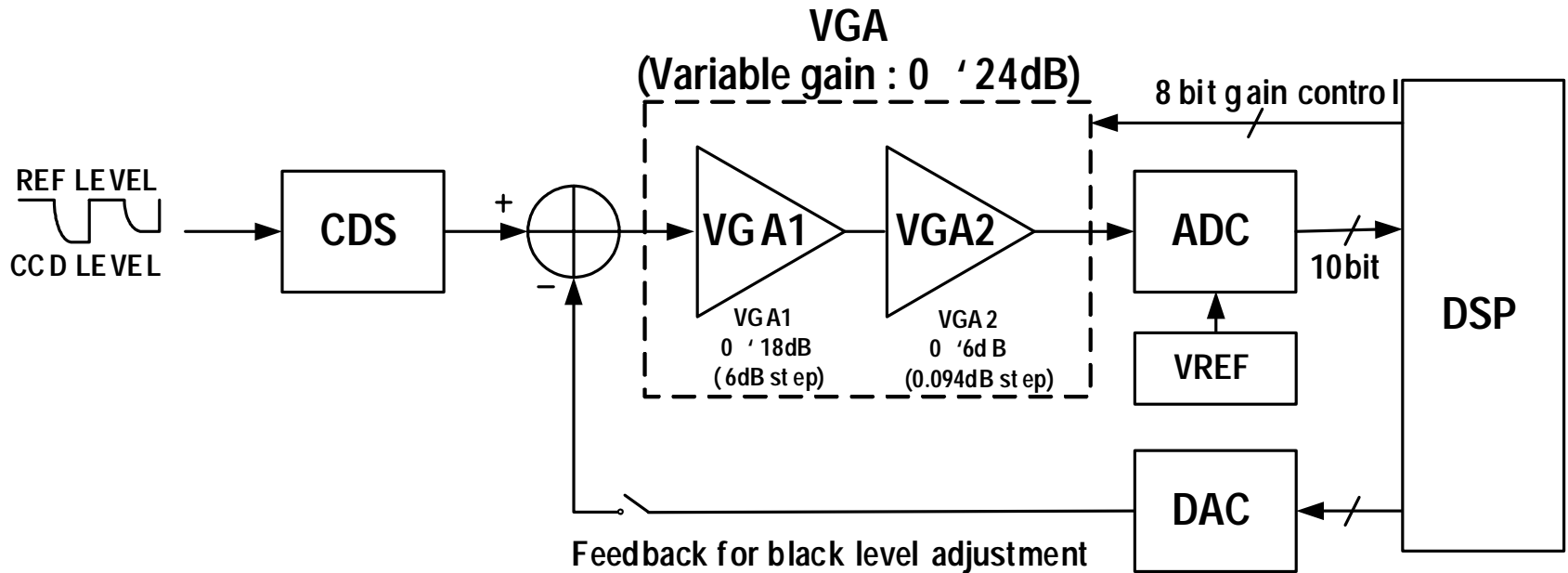
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Outline of Presentation

1. Analog/Digital Interface for CCD Image Sensor
2. Conventional Variable Gain Amplifier(VGA)
3. Proposed VGA
4. VGA design and Circuit Implementation
5. Measurement Results
6. Conclusions

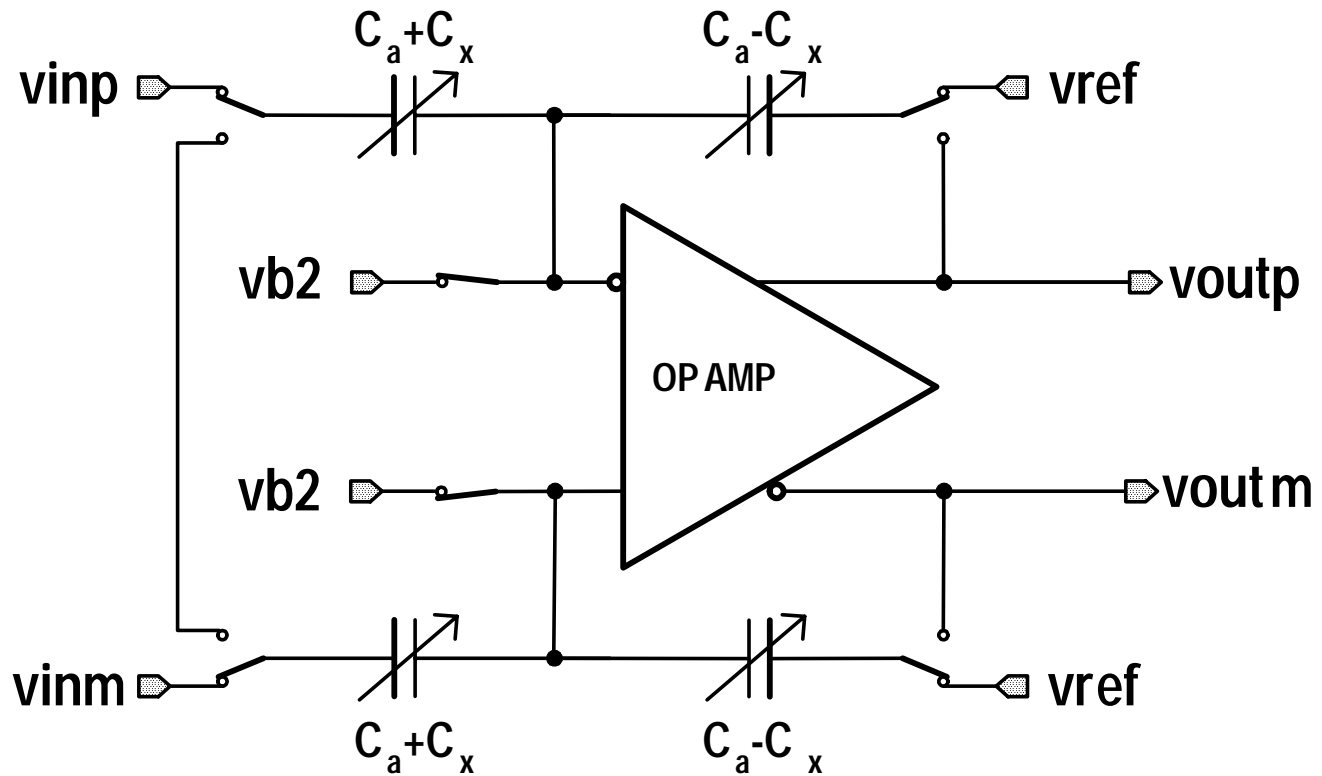
Analog/Digital Interface for CCD Image Sensor



Requirement for VGA

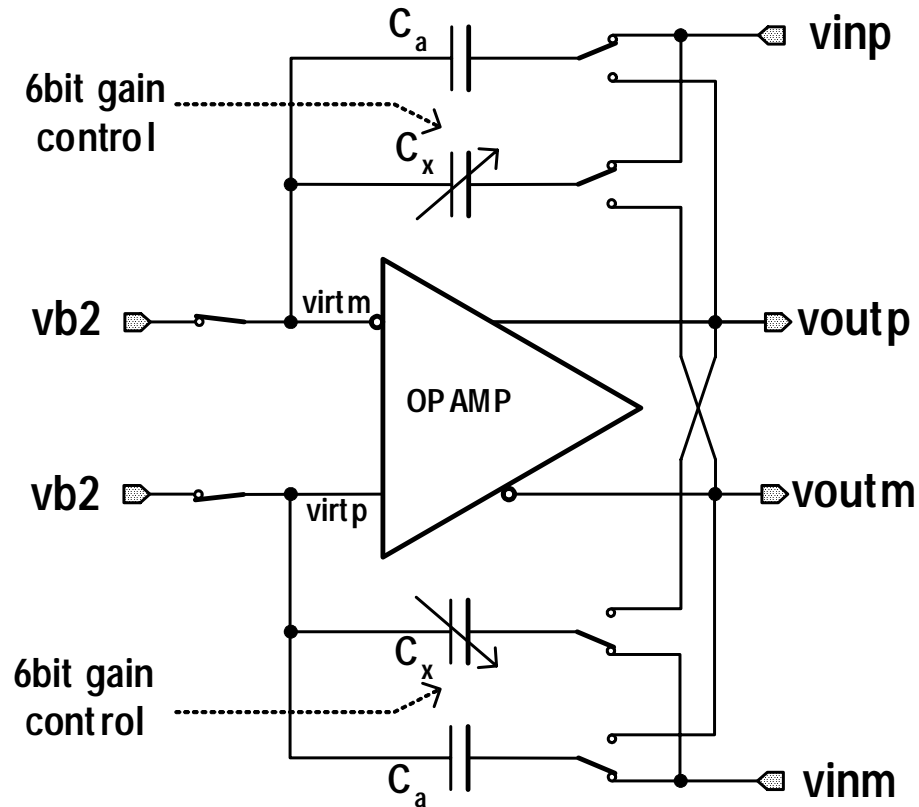
- Exponential gain control
- 8 bit gain control
- Gain range 0 ~ 24 dB (0.094 dB step)

Conventional Architecture



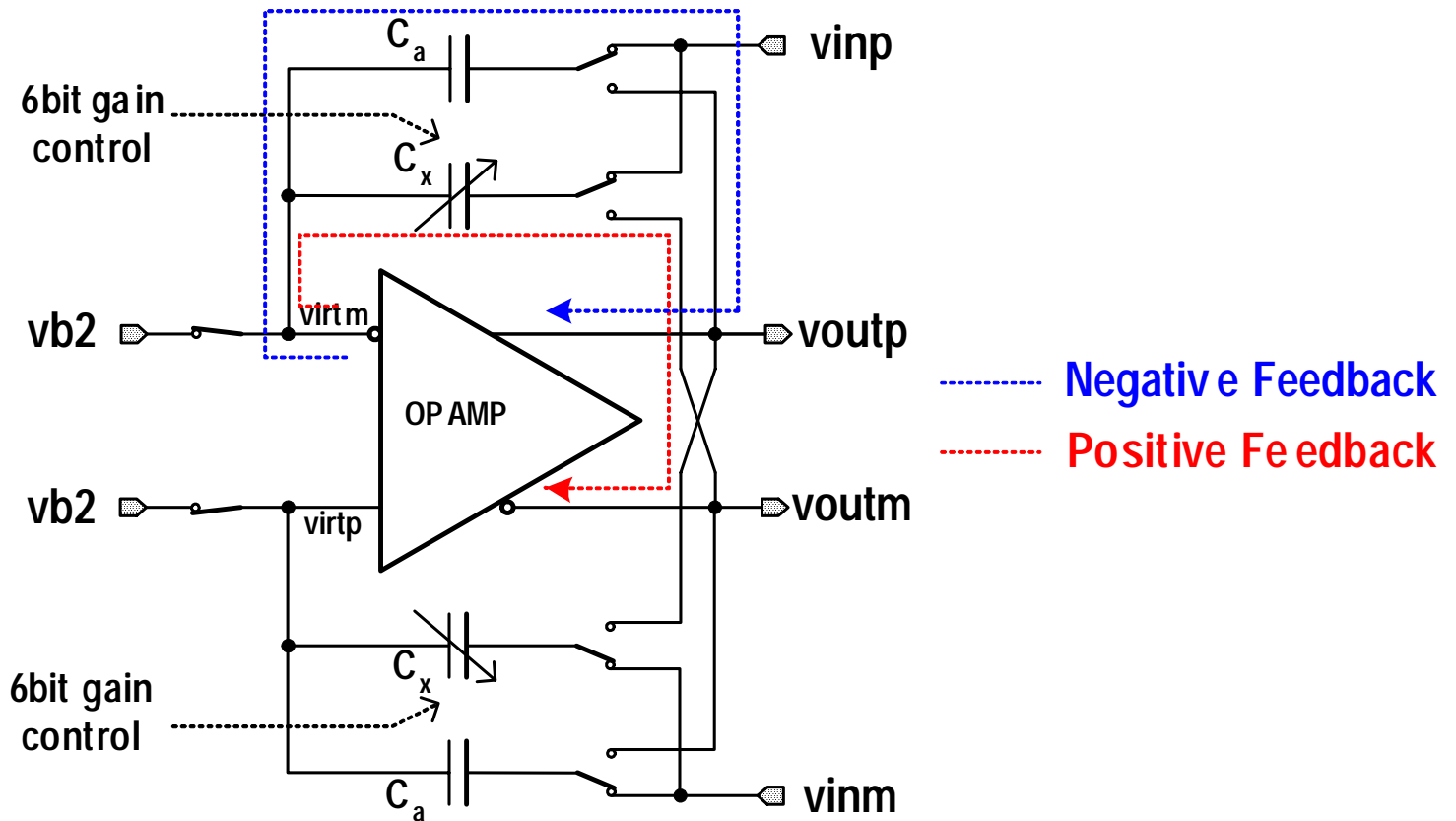
$$Gain = \frac{C_a + C_x}{C_a - C_x} = \frac{1 + x}{1 - x} \sim e^{2x}$$

Proposed VGA Architecture



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Proposed VGA Architecture



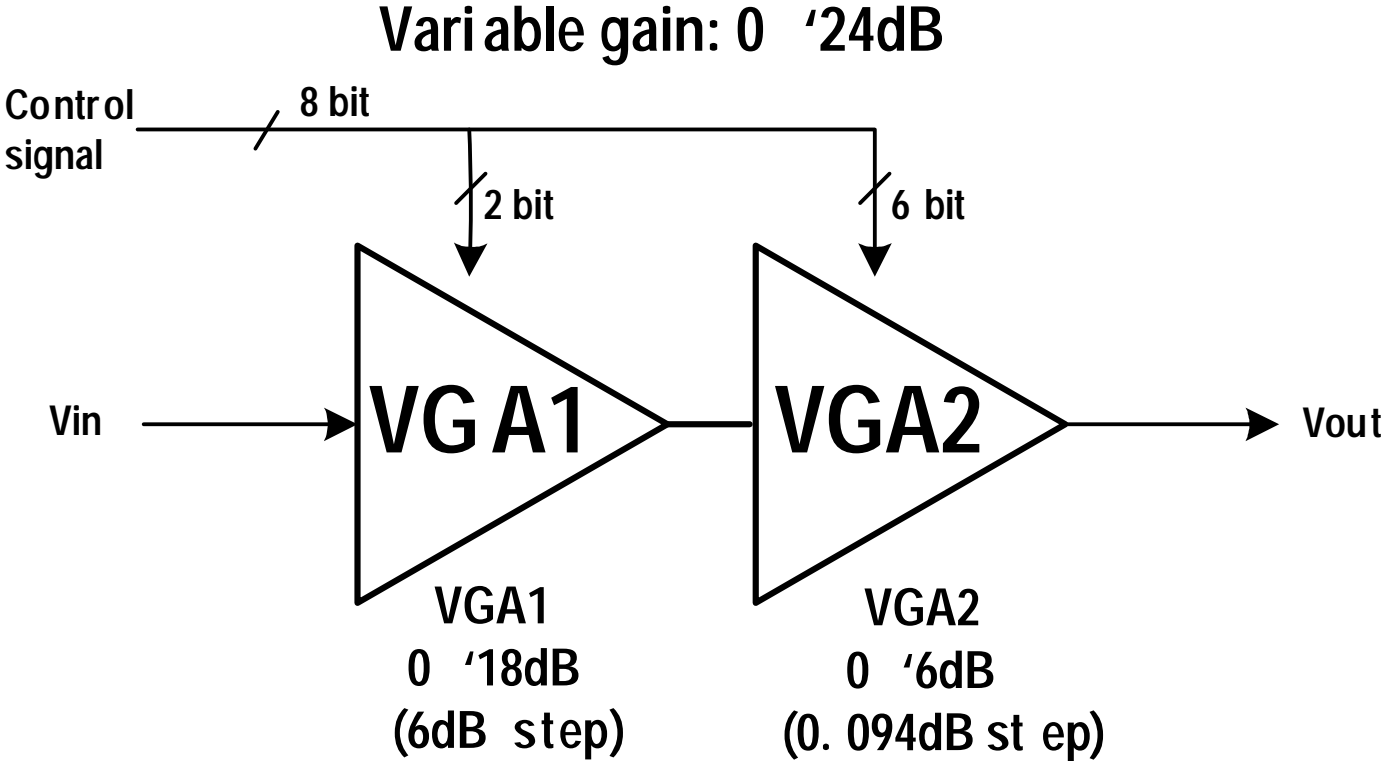
$$Gain = \frac{C_a + C_x}{C_a - C_x} = \frac{1 + x}{1 - x} \sim e^{2x}$$

Architecture Comparison

	Proposed Architecture	Conventional Architecture
Feedback Factor β	$\frac{1 - C_x / C_a}{1 + C_x / C_a} >$	$\frac{1 - C_x / C_a}{2}$
Output referred noise (V ² /Hz)	$2kT \frac{C_a + C_x}{(C_a - C_x)^2} <$	$2kT \frac{2C_a}{(C_a - C_x)^2}$

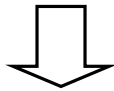
- + Larger bandwidth
- + Lower kTC noise

VGA design



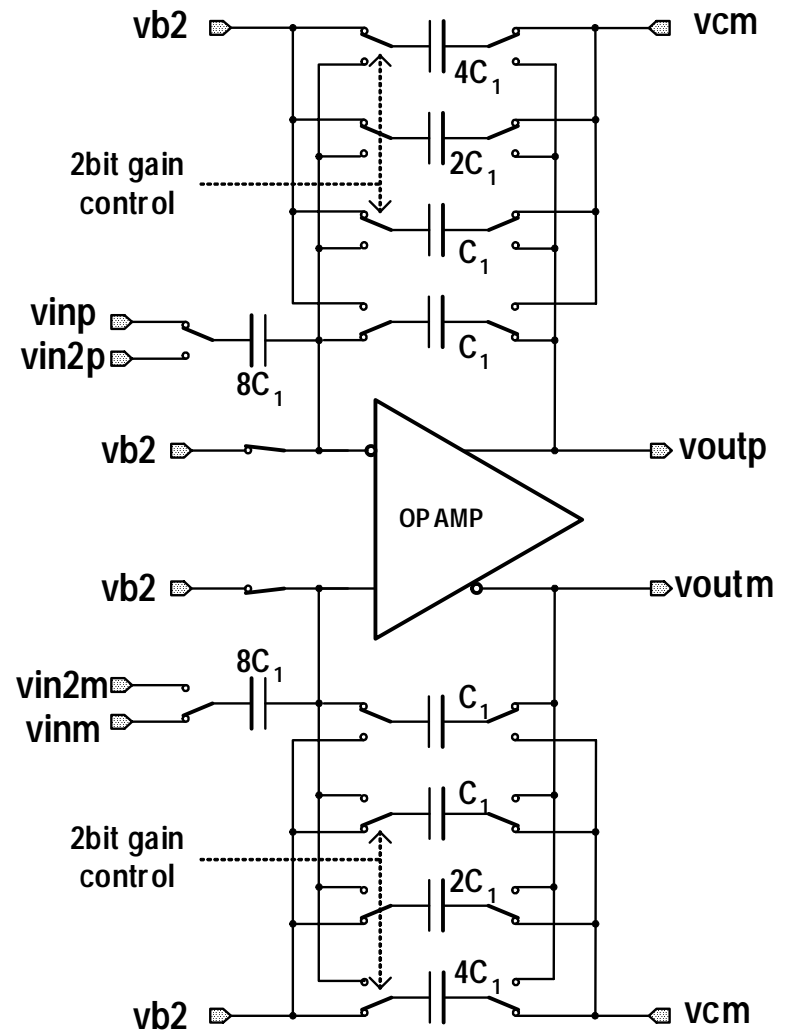
VGA design: VGA1

1. Usual SC circuit
2. Gain = 0, 6, 12 or 18 dB



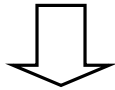
$$C_s = 8C_1$$

$$C_f = 8C_1, 4C_1, 2C_1 \text{ or } 1C_1$$



VGA design: VGA2

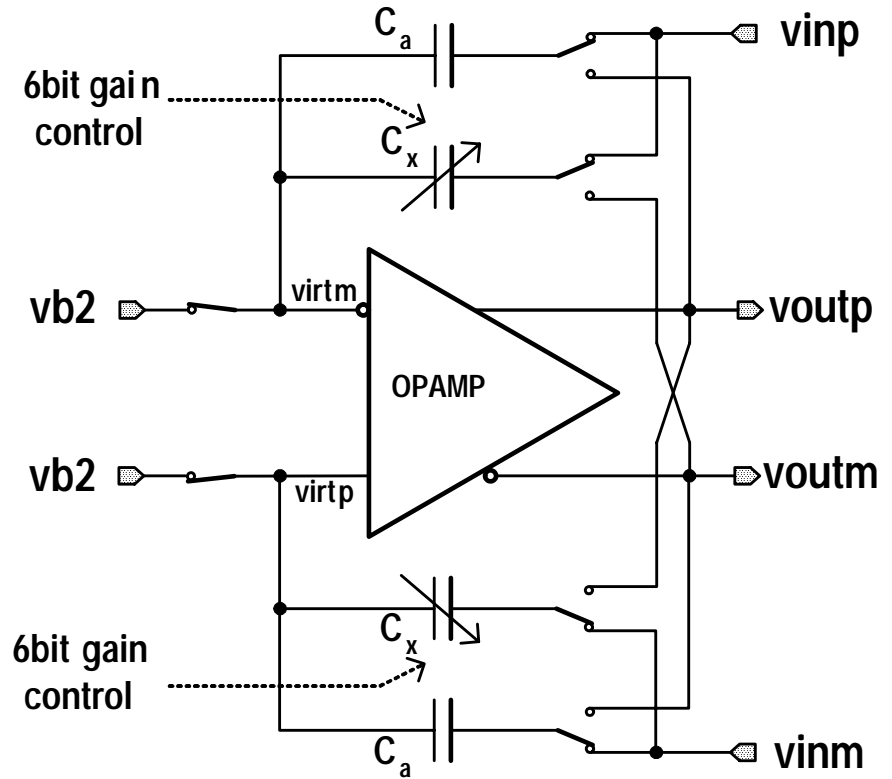
Gain = 0 ~ 6 dB
with 0.094 dB step



Variable Capacitor

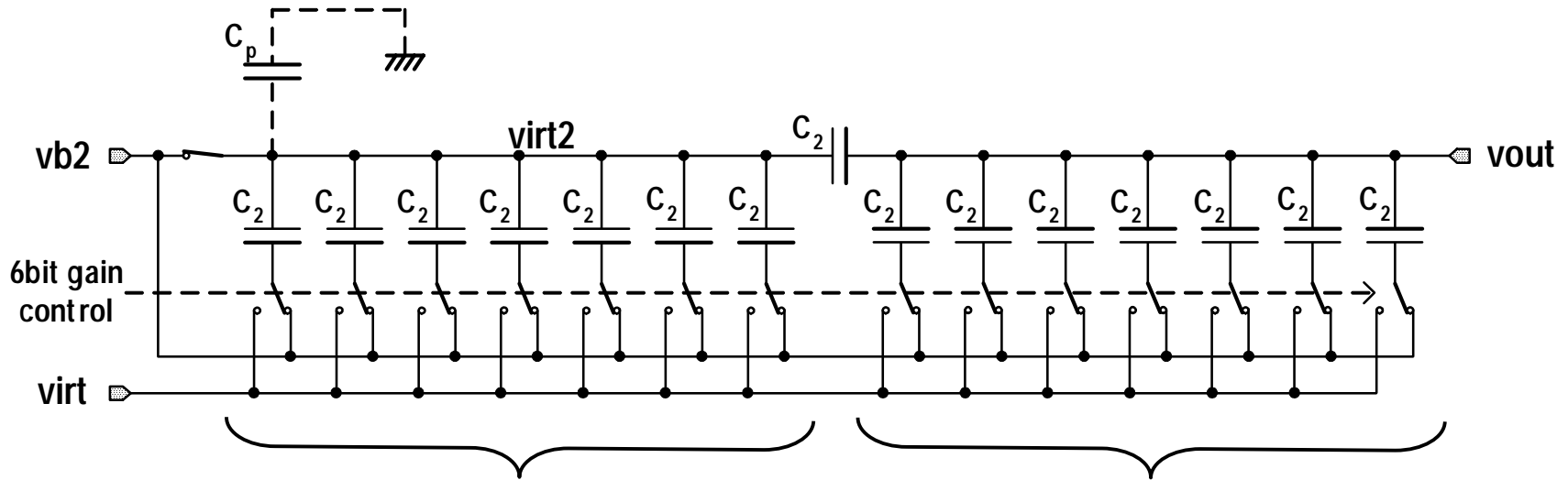
$$C_x = 0 \sim \frac{1}{3} \cdot C_a$$

with $\frac{1}{192} \cdot C_a$ step



$$Gain = \frac{C_a + C_x}{C_a - C_x} = \frac{1+x}{1-x} \sim e^{2x}$$

Variable Capacitor C_x



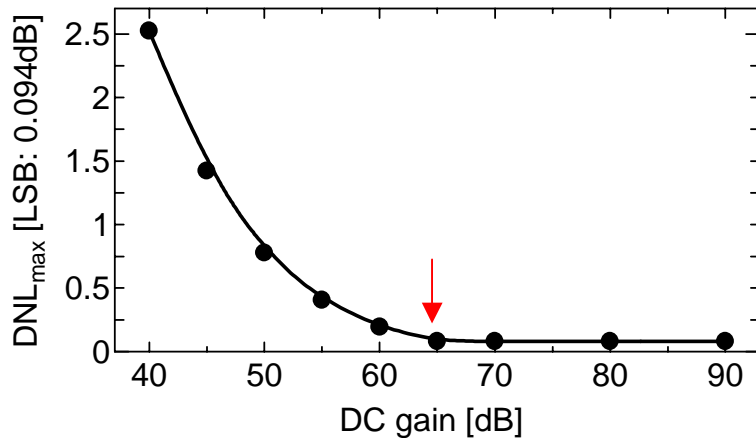
$$C_x = \frac{1}{8} n_{2a} \cdot C_2 + n_{2b} \cdot C_2$$

$$n_{2a} = 0, 1, \dots, 7$$

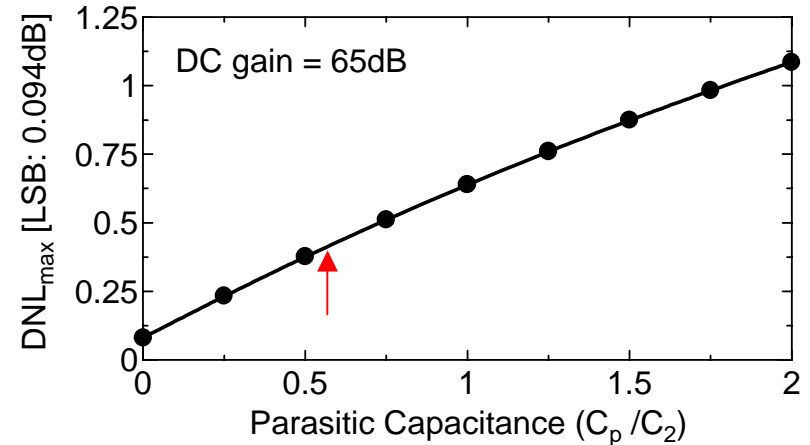
$$n_{2b} = 0, 1, \dots, 7$$

Simulation Results

DNL Dependence
on DC gain of the opamp



DNL Dependence
on Parasitic Capacitance C_p

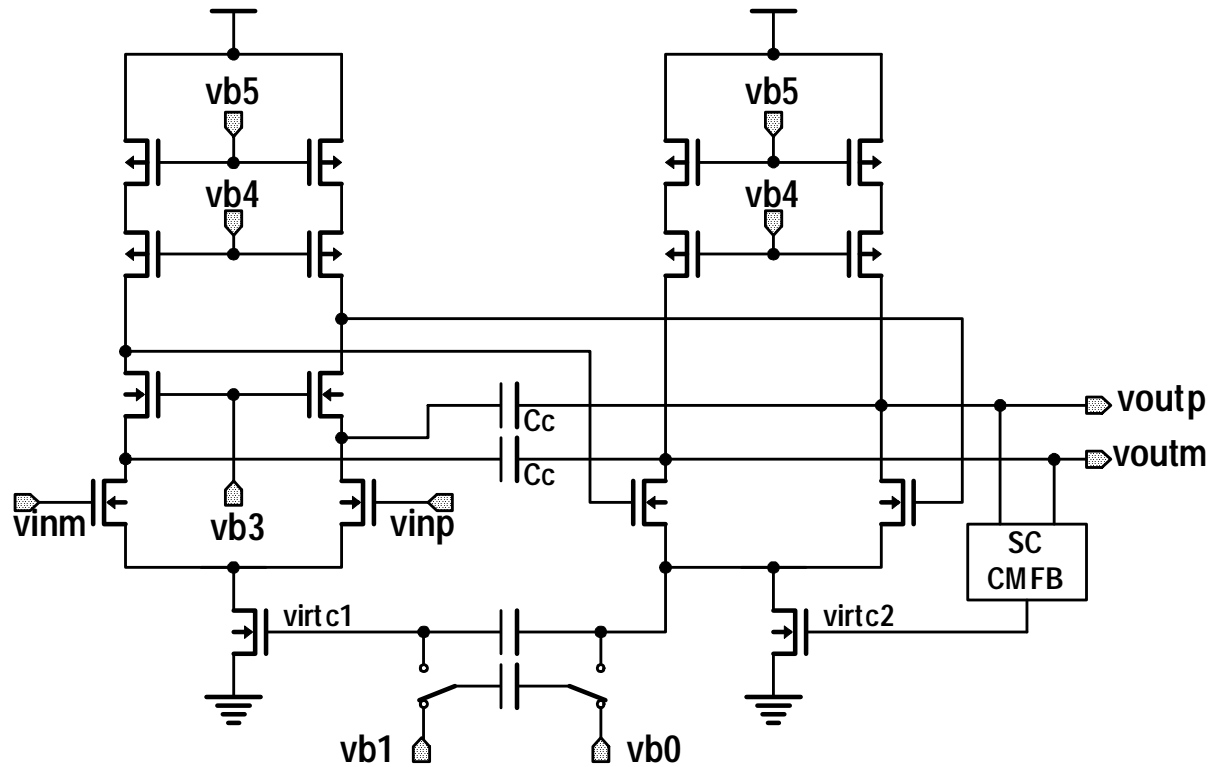


Design target

DC Gain > 65 dB

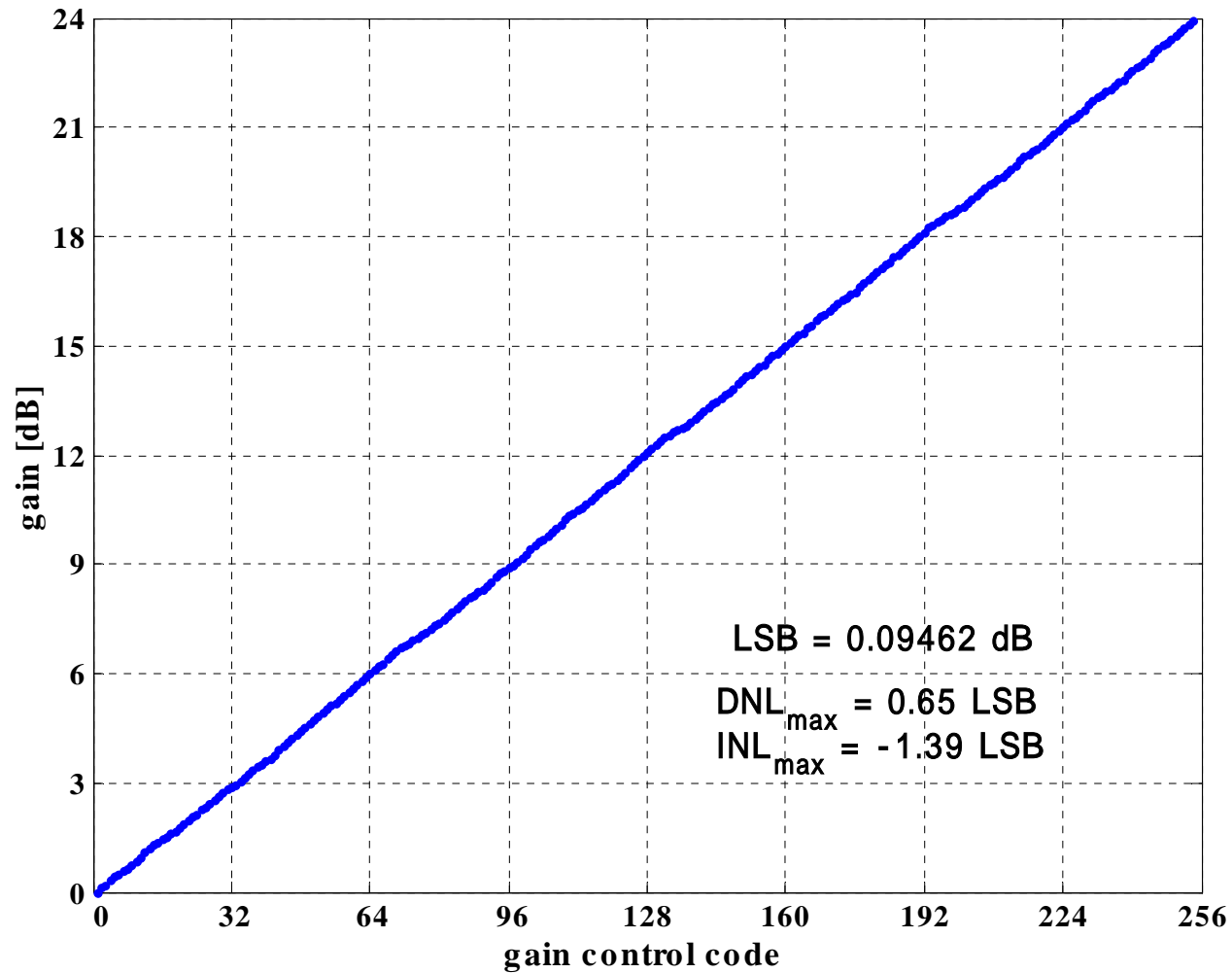
$C_p < 0.6 C_2 = 0.03 \text{ pF}$ ($C_2 = 0.05 \text{ pF}$)

Operational Amplifier

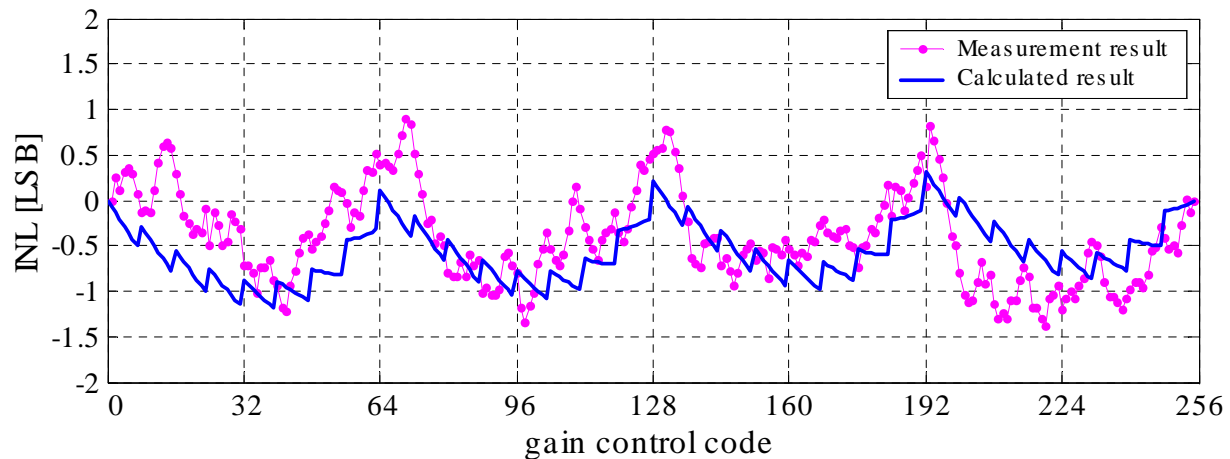
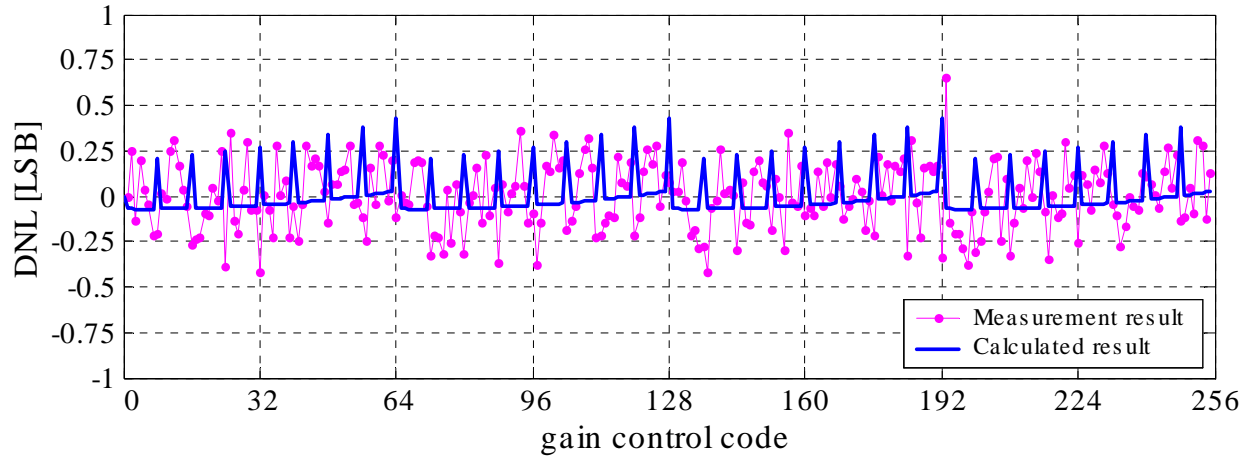


Simulated DC gain = 98 dB

Measurement Result



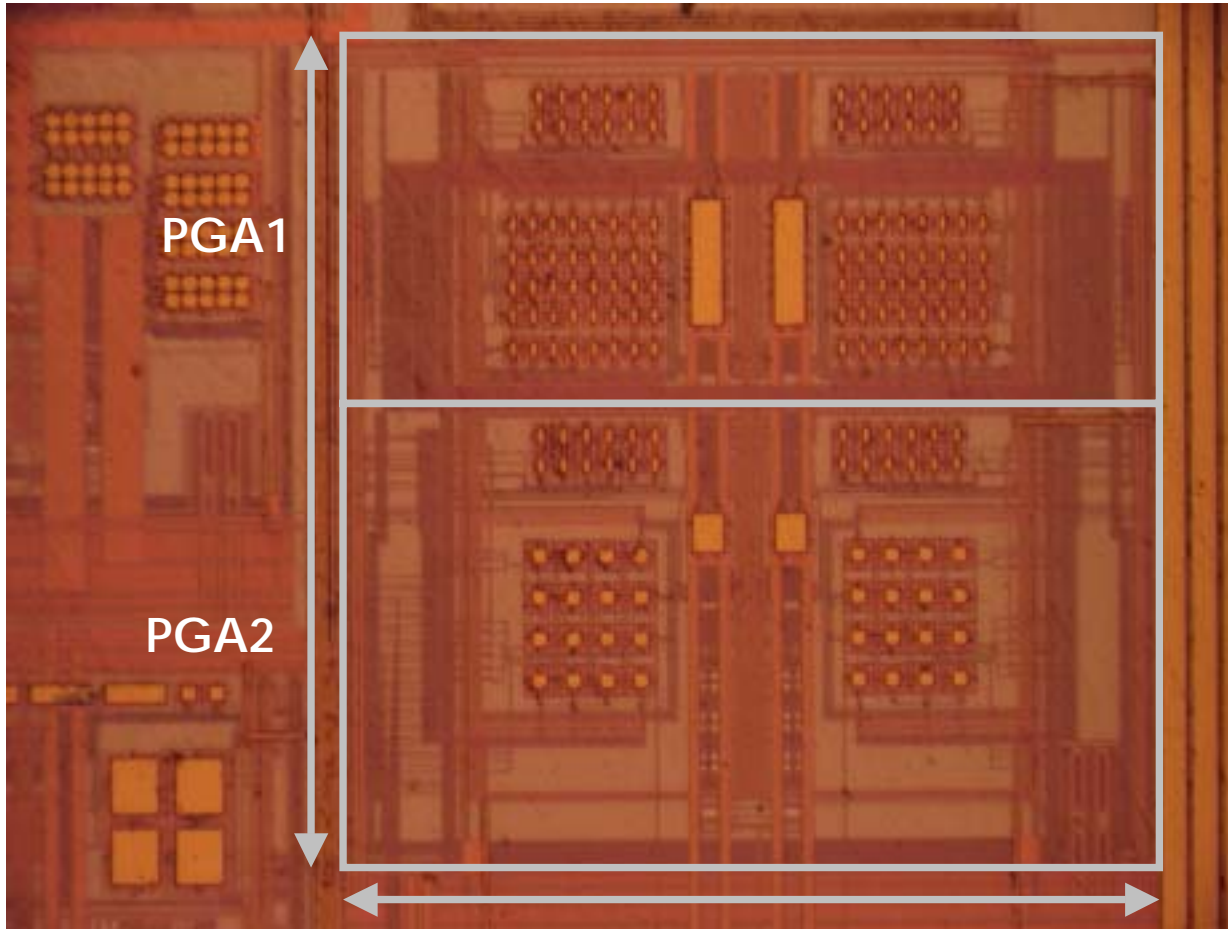
Measurement Result



Performance and Specification Summary

Sampling Rate	8 MS/s
Input referred noise	207 μ V
VGA gain range	0 ~ 24 dB
VGA gain step	0.0946 dB
VGA Gain Linearity(DNL)	0.65 LSB
ADC linearity(DNL, INL)	0.68 LSB, 1.79 LSB
Input range of ADC	2.2 Vpp, differential
Power dissipation of VGA	5 mW@2.8V
Power dissipation of ADC	15 mW@2.8V
Technology	0.25 μ m CMOS
Chip size	0.55 mm x 0.45 mm

Die Photograph



0.55 x 0.45 mm

Conclusion

Proposed variable gain amplifier

- exponential gain control with fine gain step
- First order approximation

$$e^{2x} \sim \frac{1+x}{1-x}$$

- Using a positive feedback
as well as a negative feedback
- Compact variable capacitor array
- larger bandwidth
- lower noise