

Modeling and Experimental Verification of Substrate Noise Generation in a 220Kgates WLAN System-on-Chip with Multiple Supplies

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Abstract

With increasing clock frequencies and resolution requirements in mixed-mode telecom circuits substrate noise is becoming more and more a major obstacle for single chip integration. At higher frequencies, the substrate noise is not scaling with the clock frequency anymore, especially when ringing occurs in the spectrum of the supply current transfer function to the substrate. In this paper, we propose a technique to estimate the substrate noise transients and its frequency spectrum on large telecom ASICs. The results have been verified with substrate noise measurements on a real-life test case: a 220Kgates telecom system-on-chip (SoC) implemented in a 0.35 μ m CMOS process on an EPI-type substrate.

1. Introduction

Substrate noise generated by large digital circuits degrades the performance of the analog parts on mixed-mode telecom ASICs [1]. It is important to estimate the substrate noise as it can be used for the frequency and time planning of a front-end and also for decreasing the supply bounce of a stand-alone digital design.

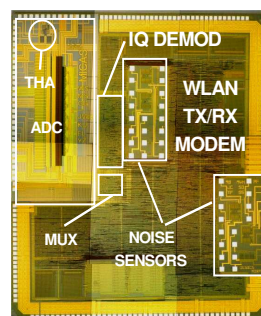
Accurate simulation of substrate noise generation depends on how well the noise sources are estimated as well as their corresponding transfer function to the substrate [2][3]. For the methodology in [3], a difference of less than 10% between the measured and simulated RMS values of the substrate noise transients for an 86Kgate digital ASIC was demonstrated. This work was limited to the noise generation by a digital multi-rate channel selection filter, not a complete mixed-mode high-performance telecom SoC. For a mixed-signal SoC, a practical modeling approach is presented in [4] to estimate the substrate noise in a Bluetooth radio chip. However, this work is limited to a scaled substrate model of an inverter only, where the direct/return current paths are neglected in a chip with multiple supplies. In reality, a chip will always have multiple supplies due to the supply pads necessary to meet the current density specs. Multiple supply regions together with the core cells, I/O pads define a complete chip-level substrate model. The model presented in this paper accurately estimates the multiple resonance frequencies, at which the substrate noise increases significantly.

To our knowledge, this is the first time that substrate noise measurements on complete high-performance tele-

com ASICs of this complexity have been published. We designed and measured a 220Kgates mixed-signal, telecom SoC, fabricated in a 0.35 μ m CMOS process on an EPI-type substrate in order to demonstrate an OFDM-WLAN modem and to measure the generated substrate noise during different operating modes of the receiver.

2. WLAN test chip description

The test chip contains an OFDM-WLAN (orthogonal frequency division modulation wireless local area network) modem [5], a low-IF digital IQ (de)modulator [6], and an 8-bit embedded ADC [7]. It also contains a substrate noise sensor [3], which is a differential amplifier with one input capacitively coupled to the quiet ground and the other input capacitively coupled to the substrate and with 3dB amplification from 20kHz to 1GHz. The chip has been fabricated in a 0.35 μ m CMOS process on an EPI-type substrate. The resistivity and the thickness of the EPI-layer are 10 Ω cm and 4 μ m respectively. The resistivity and the thickness of the conductive p+ substrate are 10m Ω cm and 400 μ m respectively. The die has been placed on a 176pin CPGA package where an average value of 8nH+0.8 Ω is measured for a single I/O pin.



Specifications

Technology	CMOS 0.35 μ m
Substrate type	EPI (10 Ω cm for EPI, 10m Ω cm for bulk)
Gate complexity	220K gates
Chip area	29mm ²
Package	176pin CPGA
Clock frequency	60MHz

Figure 1. The test chip and its specifications

The chip can be operated as either transmitter or receiver. The communication link is formed between two ASICs as shown in Figure 2, which is based on a burst communication where the data are sent in packets. The sequence of the operating modes of this communication is shown in Figure 3. After master reset (RESET), the chip starts in STAND_BY. In this mode, the clocks in the modules are all enabled (see Figure 2). An external micro-controller programs the parameters and the burst data.

Then it enables the communication (RX_START). The clocks of the modules are all disabled (via gating) until the synchronization data is received (SYNC_OK). After synchronization the data go through the modules such that the datapath pipeline is fully used (DATAPATH_OK). The received data is recorded by the microcontroller via output I/Os (RX_OUTPUT). After the completion of the burst, the chip goes into STAND_BY mode automatically.

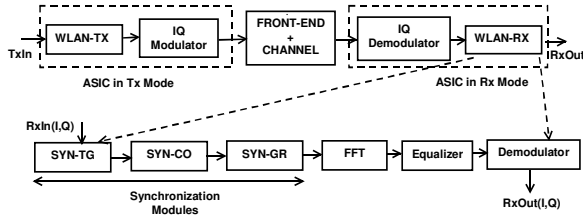


Figure 2. Transmitter and receiver link in WLAN SoC

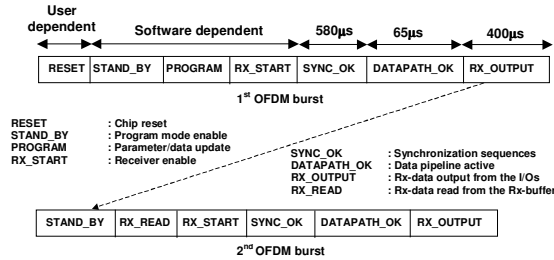


Figure 3. The operating modes of the receiver

3. Substrate macro model of WLAN SoC

On a typical p-type substrate the noisy supply (Ldi/dt noise) couples into the substrate capacitively from VDD via the n-well junction capacitor and resistively from VSS via the substrate contacts. Fast switching outputs (CdV/dt noise) couples into the substrate via the diffusion capacitor. Previous work [3] presents an experimentally verified high-level substrate noise simulation methodology for low-ohmic EPI-type substrates taking into account these mechanisms, where they are modelled using two current sources, the bulk and supply current, with the impedances between VDD, VSS and the substrate.

The chip-level substrate network of the test chip is constructed using the substrate macro models of the core, and of the I/O and supply pads taking multiple supply regions into account. The test chip consists of three digital supply regions: IQ (de)modulator (FIL), multiplexing (MUX) and WLAN baseband modem (WLAN). For each of those supply regions, the assignment of the cells, the supplies and the I/O pads is listed in Table 1. The chip-level substrate model used for the substrate noise simulations is shown in Figure 4. For the used low-ohmic EPI-type substrate, the substrate forms a common node in the conductive p+ substrate. Therefore, the substrate macro models for the core, I/O and supply pads for each supply region can be combined in parallel together with the supply and bulk current sources. Table 2 shows the element values computed, using the methodology in [3], for this parallel combination. Note that the impedance between VSS and

the substrate is less than $51m\Omega$ such that all VSS noise appears directly in the substrate.

Features	FIL	MUX	WLAN	Total
Core area in gates	12192	2631	157823	172646
Flip-flops	408	185	6131	6724
Posedge flip-flops	331	152	5994	6477
Negedge flip-flops	77	33	137	247
Core supply pairs	2	2	7	11
I/O supply pairs	N/A	5	3	8
Input pads	N/A	32	15	47
8mA output pads	N/A	3	N/A	3
4mA output pads	N/A	27	N/A	27
4mA bidir pads	N/A	N/A	16	16
Clock frequency	f_{system}	f_{system}	$f_{system}/3$	f_{system}
Clock duty cycle	50%	50%	67%	50%
Max clock skew	50ps	50ps	156ps	206ps

Table 1. Features of different supply regions in WLAN SoC

In order to simulate the substrate noise generation, one has to also estimate the main noise current sources in the chip-level substrate model. These model the supply and bulk currents from the core and I/O cells separately.

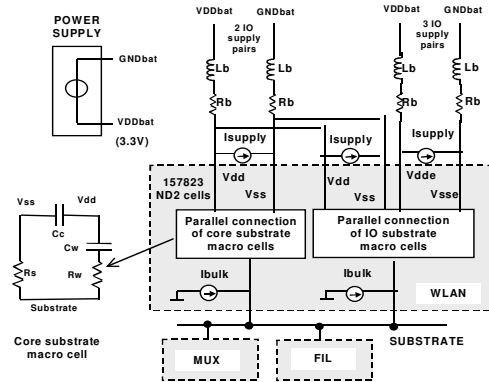


Figure 4. Chip-level substrate model for WLAN SoC

Elements	FIL	MUX	WLAN	TOTAL
R_s	0.727Ω	3.368Ω	0.056Ω	0.051Ω
C_w	$132pF$	$29pF$	$1.708nF$	$1.869nF$
R_w	0.826Ω	3.827Ω	0.064Ω	0.058Ω
C_c	$110pF$	$24pF$	$1.424nF$	$1.558nF$

Table 2. Element values of the core models in WLAN SoC

For synchronous CMOS circuits, the current sources can be approximated by a triangular waveform (see Figure 5a). The total spectral energy of the supply current decreases by decreasing its energy and/or the rise/fall time in the time-domain (see Figure 5b). This will also reduce the generated substrate noise, as the RMS value of the substrate noise is proportional to its spectrum integral. It is therefore important to correctly estimate the peak value and rise/fall time of the supply current. For each supply region the triangular supply current has been computed accordingly taking into account: (1) the probability of switching flip-flops/logic; (2) average load due to the fanout and the interconnect; (3) the clock skew.

To estimate the supply current, one has to know the average amount of simultaneous switching activities during an operating mode. In a first experiment to compare the measurements with simulations, the chip has been simulated in the STAND_BY operating mode where the chip

has been configured with default values, and no input is applied except the clock. Within this regime, the switching activity of a flip-flop is dominated (around 92% of all flip-flops) with switching clock inputs only. The amount of switching logic except the clock buffers and the flip-flops is computed to be less than 10% of the total switchings based on the switching statistics from the simulations. The supply current waveform of the core cells is obtained by scaling the current of a single flip-flop driving a single two-input NAND gate. The bulk current is also derived in a similar way. Figure 5c shows the values of the peak and the rise/fall time of the supply currents.

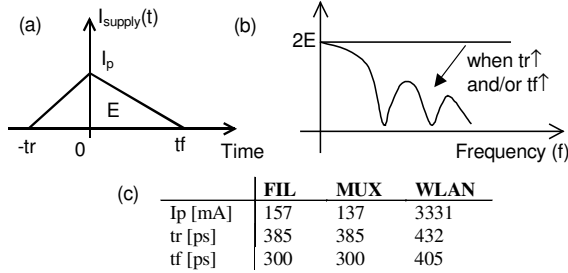


Figure 5. Supply current with triangular approximation: (a) time domain (b) frequency domain (c) computed values

4. Experimental Results

4.1. WLAN SoC substrate noise measurements

At all the measurements, the data have been recorded by measuring the differential output of the substrate noise sensor via a probe with a bandwidth of 500MHz and a sampling scope. Different operating modes of the receiver (see Figure 3) cause a different number of switching activities, and therefore different substrate noise levels. The link has been configured as shown in Figure 2 at 10MHz clock (50% duty cycle). Table 3 shows the measured values of the generated substrate noise for different operating modes. A change from SYNC_OK to DATAPATH_OK causes a measured increase of 7% in the RMS value of the substrate noise. This increase is due to the enabled modules, such as the FFT and the equalizer, after the synchronization acknowledgement. An increase of 44% is measured in the peak-to-peak value of the substrate noise for a change from DATAPATH_OK to RX_OUTPUT even if the number of the switchings caused by the core cells is the same. This increase is mainly due to the additional switching of 6 output I/Os where each one is loaded with 12pF in parallel with 100kΩ. The measured noise increases when the loads driven by these I/Os are increased.

Operating Region	VSUBpp [mV]	VSUBrms [mV]	% of RMSmax
RESET	100	16.9	47%
STAND_BY	197	27.4	76%
PROGRAM	213	27.9	78%
RX_START	228	30.4	84%
SYNC_OK	220	29.7	83%
DATAPATH_OK	235	33.2	92%
RX_OUTPUT	338	36.0	100%

Table 3. Measured substrate noise versus operating modes

Figure 6 shows the measured peak-to-peak (a) and RMS (b) values of the substrate noise versus the clock frequency in the STAND_BY operating mode. At operating frequencies of 1.5 MHz, 14MHz, 35MHz, and 76MHz, the substrate noise shows some local peaks. Measurements show a linear relationship between substrate noise and the supply voltage (see Figure 7).

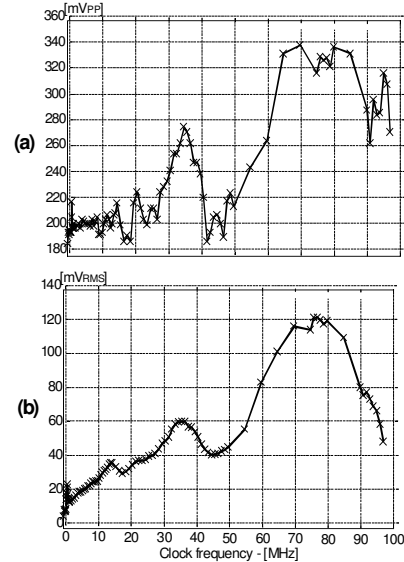


Figure 6. Measured substrate noise versus clock frequency: (a) Peak-to-peak, (b) RMS values

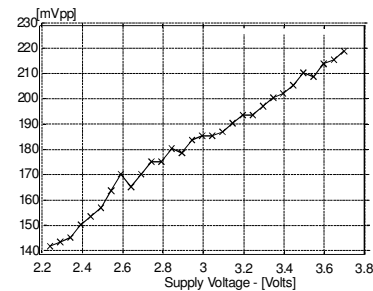


Figure 7. Measured substrate noise versus supply voltage

For WLAN applications, a high-speed, high-accuracy (10-bit) Nyquist ADC is required. However, substrate noise degrades its resolution and dynamic properties. The effective number of bits (ENOB) drops for increasing input signal frequencies especially at the clock harmonics. For the WLAN SoC the worst case substrate noise is achieved in the RX_OUTPUT operating mode. If this circuit is operated at a 60MHz clock rather than 10MHz, the measured substrate noise in this mode increases from 338mVpp to 473mVpp since the clock frequency approaches the major resonance of the circuit (see Figure 6a). For an embedded 10-bit flash ADC having an input swing of 1.3Vpp at 3V supply and running at 60MHz, the substrate noise has to be rejected as much as 51dB for a 473mVpp substrate noise. Proper shielding and separation of the analog circuit and its supply, although not very effective at low-ohmic substrates, advanced packaging (e.g. flip-chip bonding) for less inductance, and differential design techniques are crucial for higher ENOBs, in con-

junction with low-noise digital design techniques to reduce the substrate noise [8][9]. Also the ADC can be operated at the silent states of the substrate, which can be assured with proper damping of the substrate noise oscillations.

4.2. Verification of substrate macro model

In order to measure the spectrum envelope of the substrate noise; the clock frequency has been reduced down to 1 MHz. This low frequency clock will allow the triangular waveform response of the network to reach an asymptotic value before the next clock edge. On the other hand, a single cycle simulation of the substrate noise for 1000ns, which is the same as the clock period, has been performed on the network (see Figure 4), with the supply and bulk current sources of the I/O and core cells.

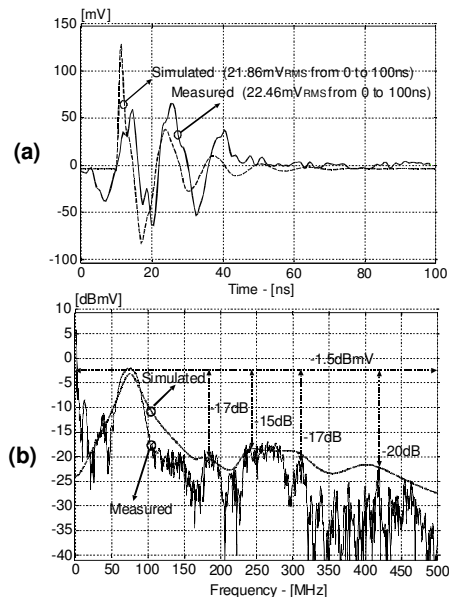


Figure 8. Measured and simulated substrate noise due to a single cycle supply current: (a) time- (b) frequency-domain

Figure 8 shows the comparison of the simulations with the measurements. As the supply current waveforms do not model the switching of the clock buffers and input capacitive coupling, the peak before the major clock edge were not estimated (see Figure 8a). The simulated waveforms are damped more than the measurements. The first sharp peak in the simulations is due to the piecewise linear approximation of the supply current (also in SPICE). In reality these sharp edges do not exist. The substrate noise has been estimated within 5% error in its RMS value computed from 0ns to 100ns. The later values show low-frequency oscillations, which were not estimated.

In the frequency domain we estimate the major peaks at 80MHz, 175MHz, 250MHz, 310MHz and 410MHz. The major resonance is at 80MHz due to the WLAN core cells. The next coming resonance (at 175MHz), which is 17.0dB below the major resonance due to the FIL core cells. The remaining resonances at 250MHz, 310MHz and 410MHz are due to the MUX core cells, the MUX I/Os, and the FIL I/Os respectively. The low-frequency peaks in the measurements are due to the PCB decoupling and traces, the power supply, and the LC-tank circuits formed between

the I/Os and their loads, which are not included in the model. The frequencies where the peak is observed in Figure 8b is the clock frequency where the substrate noise makes local maxima in Figure 6b. This shows that the spectrum estimation is important to estimate the generated substrate noise at a given clock. For reducing the major resonance, the number of supply pads assigned to the WLAN region has to be increased for less inductance. This will also shift the resonance to higher frequencies.

5. Conclusions

We have presented substrate noise measurements of a complete high-performance telecommunication ASIC (WLAN SoC) with 220K gates. The substrate noise measurement results from such SoC are useful for defining the specifications for a possible embedded analog front-end. Embedding a 10-bit ADC on this WLAN SoC with a 1.3V input swing and running at 60 MHz is a big challenge, which requires a 51dB substrate noise rejection for a worst case generated substrate noise of 473mVpp. We have experimentally verified that the scaled chip-level substrate model together with the triangular waveform approximation of the current sources efficiently estimates the generated substrate noise. We have accurately estimated the 5 major resonances and their relative magnitudes with 1.5dB relative error at the major resonance with respect to the measurements on this WLAN SoC.

6. Acknowledgements

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7. References

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