CIRCUIT EDIT THROUGH COPPER POWER PLANE WITH HALOGEN

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TECHNOLOGY AND CIRCUIT EDIT

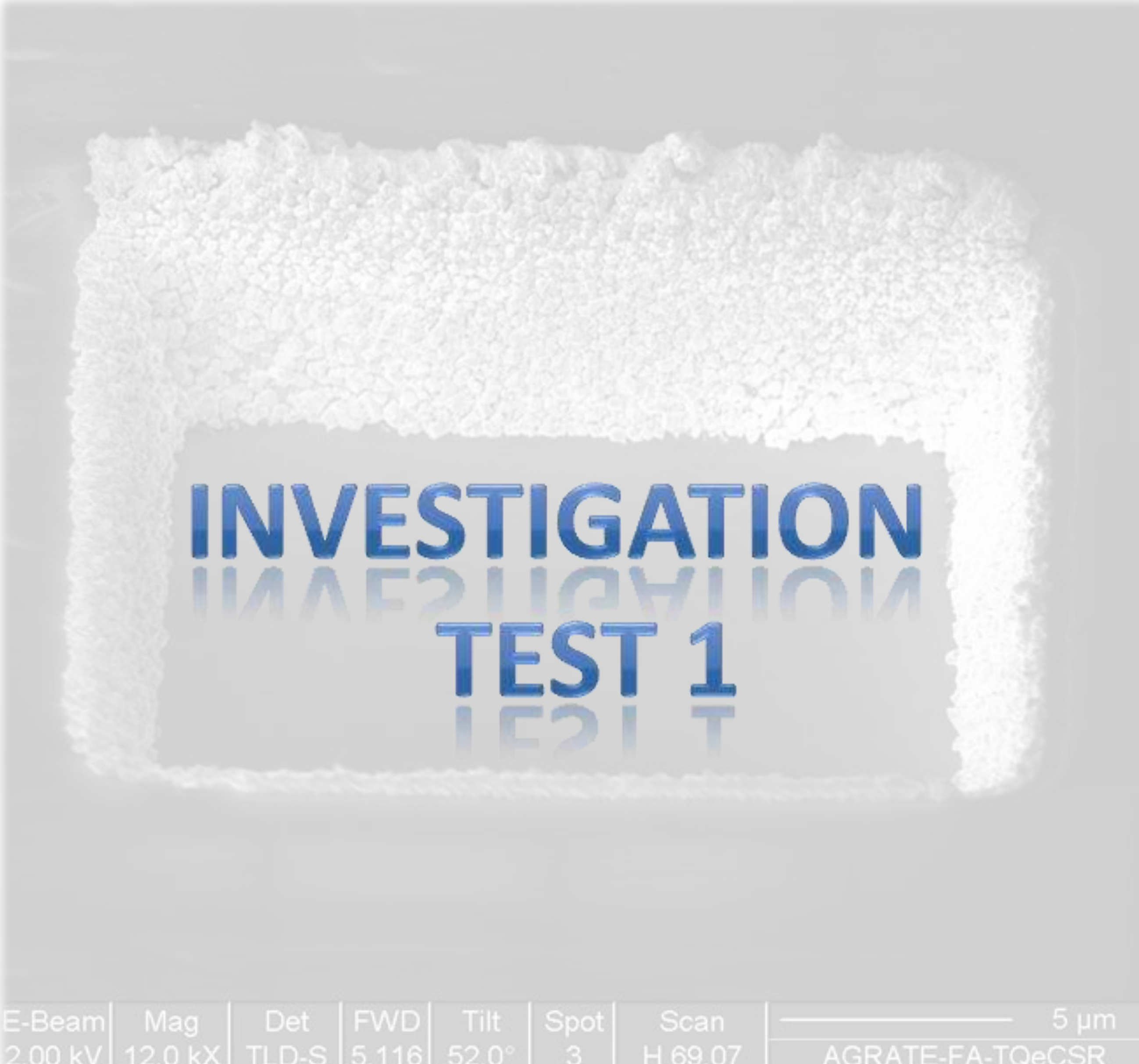
- **In an effort to enhance the performance of chip**
  - the IC industry made a switch in materials from aluminum to copper for use in metallization layers.
  - Since FIB are an integral part of *IC Debug*, *Fault-Isolation* and low *Yield Analysis*, an immediate problem was encountered when copper metal was milled in the FIB.
- **In general Cu process differs among manufactures, yields different results**
  - Therefore different FIB milling parameters are required.
- **Focused Ion Beam is tracking the evolution of IC interconnect material trends by developing**
  - application-specific chemistries.
  - circuit edit approaches
- **Continuous CE challenge**
  - Address both laterally and vertically scaling of dimensions
  - Coming soon new generation of Copper

CHALLENGES OF CIRCUIT EDIT

- **Which are the expectation on chemistries in CE?**
  - Enables different material deposition
  - Helps to improve removal while protecting surrounding materials.
  - Preferably chemistry must be passive until activated by the ion beam.
  - Spontaneous reaction is undesirable, exceptions can be contemplated:
    - XeF_2 etches spontaneously Si, but not SiO_2 (so it can be used to etch various dielectrics)
    - Heavy halogens such as Cl, Br, I etch very well Al , but spontaneously corrodes Cu

- **Copper metallization**
  - Slows down CE processes
  - Copper unlike Al has bigger grains
    - These grains etch at different rates, depending on grain orientation relative to ion beam
  - Solution to etch Copper
    - Not accelerate removal of Cu but decelerate removal of SiO2 (protect the dielectric)
    - Oxidizing Cu
    - Cut in progressive tilt mode without/without gas

INVESTIGATION TEST 1



EDI CU-BULK RECIPE

- **Goal**
  - Demonstrate the performance of the **Cu-Bulk EDI*** recipe
  - Compare results with the typical **Enhanced Copper Etch** (Cu-II) recipe
- **Recipe outline**
  - EDI (Ethylene diiodide) corrodes spontaneously exposed Cu and it is used to our benefit
    - Polycrystalline Cu gets amorphized and it loses Cu grain structure
    - Flat removal of Cu under controlled beam scanning parameters
  - Consideration on Ion Beam scanning parameters
    1. Provide enough time for chemistry to react spontaneously with Cu, to develop corrosion layer (chemistry pressure, box frame time, refresh time)
    2. Achieve a certain corroded Cu layer thickness that can be evenly removed by the ion beam (Beam current, dwell time , number of pixels)
    3. As long as corrosion layer is completely etched by each ion beam scan, the process works effectively.
  - Creating a corroded Cu layer and etching it instantly during FIB mill, provides very fast and planar copper removal.

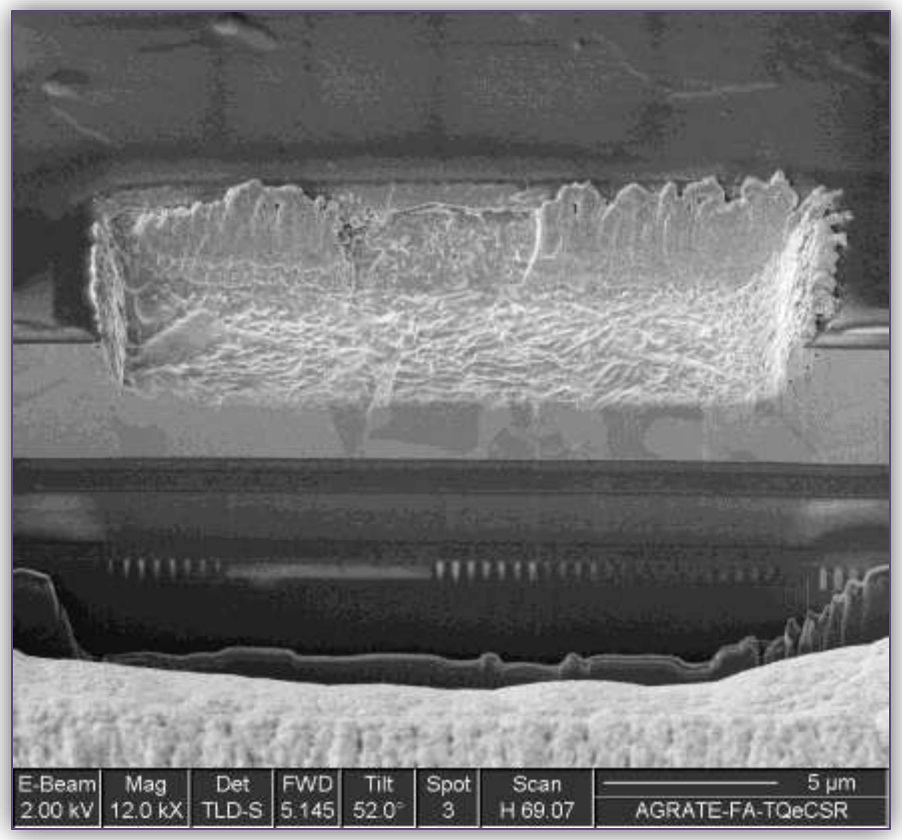
*United States Patent Application 20080113455

TEST 1: EDI CU-BULK RECIPE QUALIFICATION

- **Setup of the investigation**
  - Open 2 different trenches with
    - *EDI CU-BULK* recipe
    - *Enhanced Copper Chemistry* (Cu-II) recipe
  - Milled box area is 18x18μm^2
  - Cu power plane of 3,75µm thickness
- **Cross section analysis at SEM**

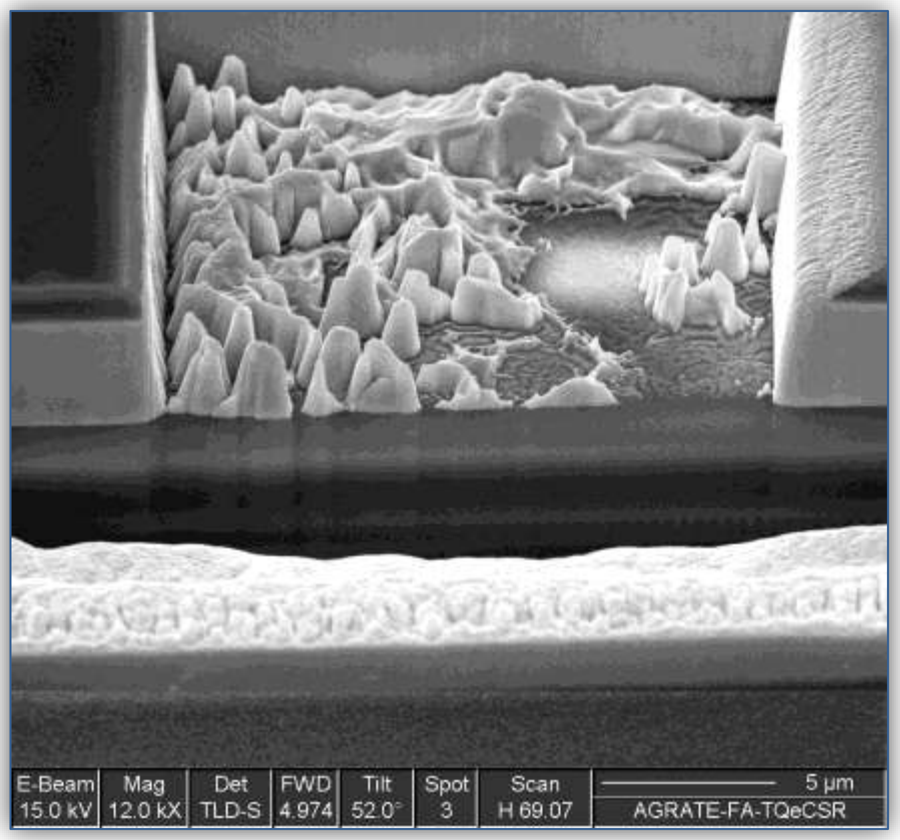
TEST 1: RECIPE COMPARISON AT HALF PROCESS

Bulk-EDI RECIPE



- 5 min recipe (half time)
- Flat removal progress

Cu-II RECIPE

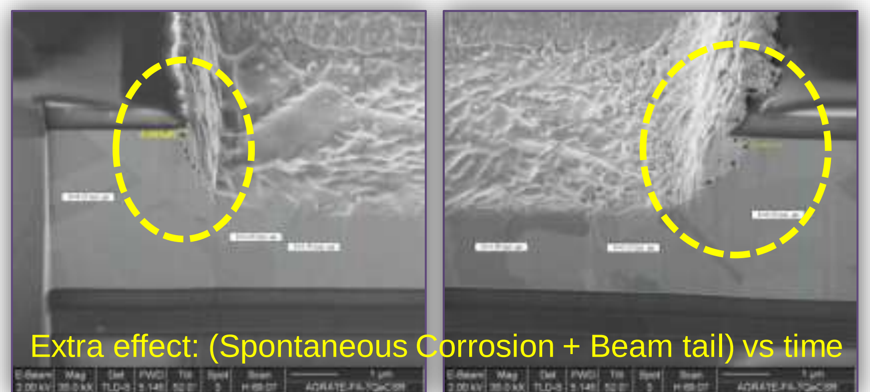


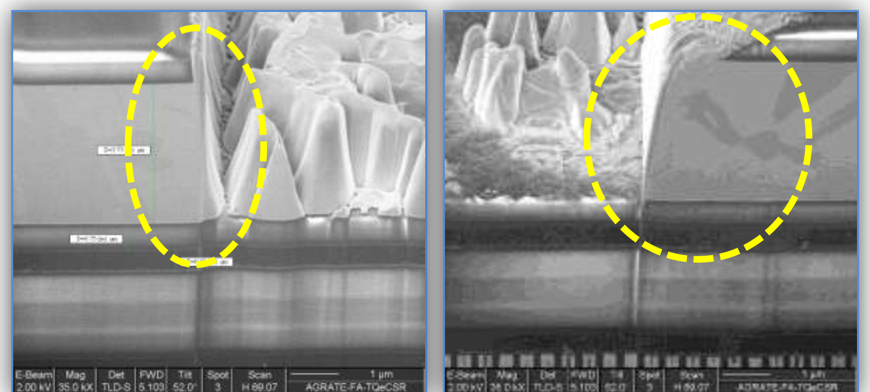
- 25min recipe (half time)
- Strong Topography, but high ILD protection

TEST 1: RECIPE COMPARISON AT HALF PROCESS

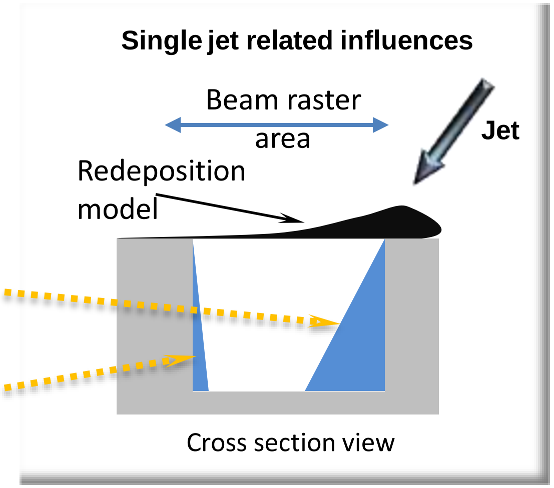
Bulk-EDI RECIPE

Cu-II RECIPE



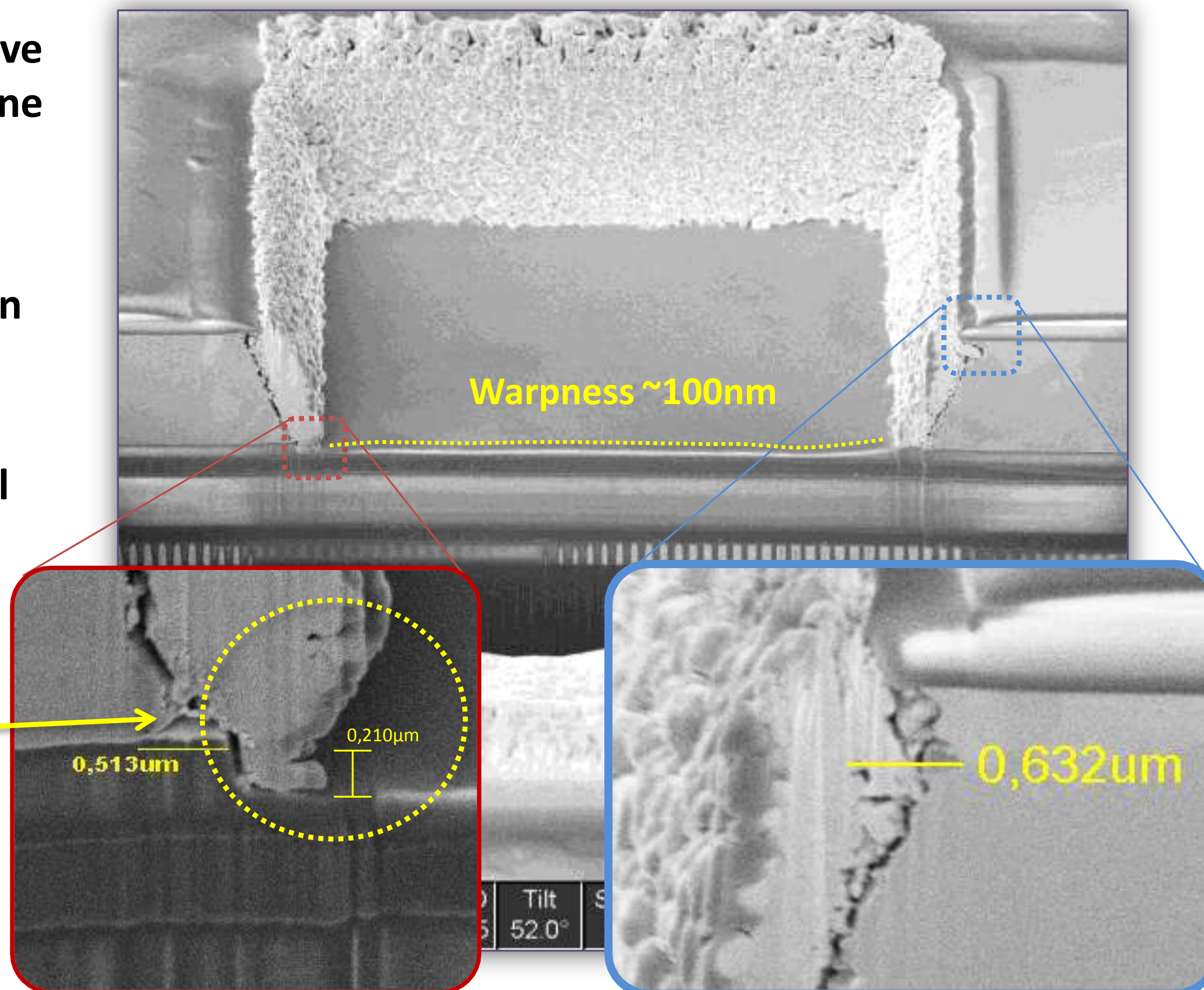


- Re-sputtered material is gas flux dependant and its redeposition appears on the jet side. The effect is influenced by gas flow rather than by beam raster.
- Side wall shadows gas flow. Reduced gas density does not give vertical wall and clean cut
- Higher gas provides steeper side walls and clean cut.



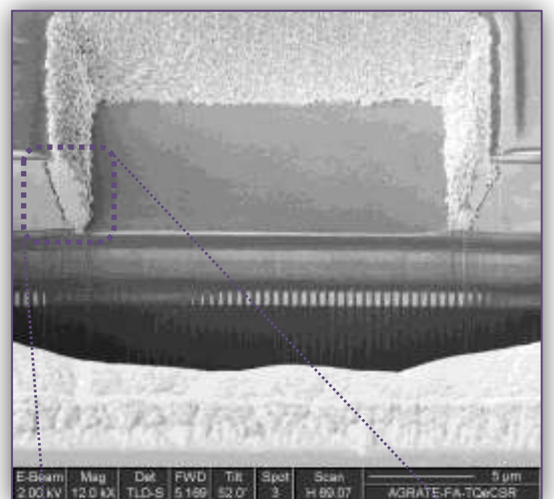
TEST 1: VIEW OF THE CUT WITH BULK-EDI RECIPE

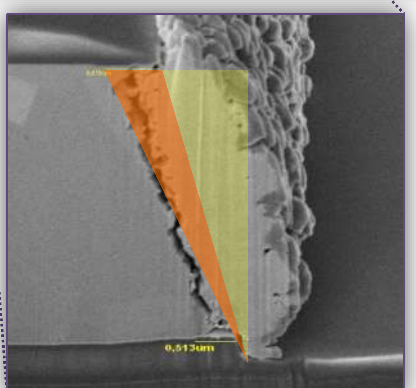
- **10 min of recipe to remove 3,75 µm of Cu power plane**
- **Flat and clean Cu power plane removal**
- **Under the top passivation the sidewall overetch is ~632nm**
- **ILD overetch over the full trench is ~210nm (ILD is 500nm)**
- **View of the amorphization progress above etched area**



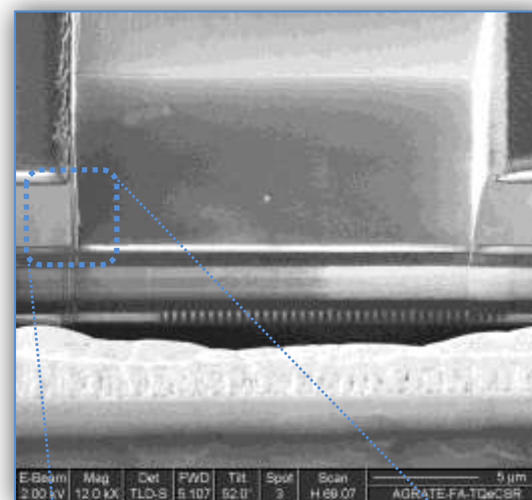
TEST 1: RECIPES COMPARISON AT THE END

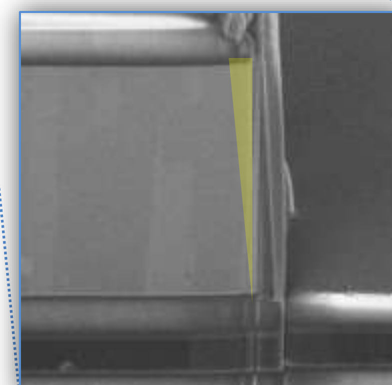
Bulk-EDI RECIPE vs Cu-II RECIPE



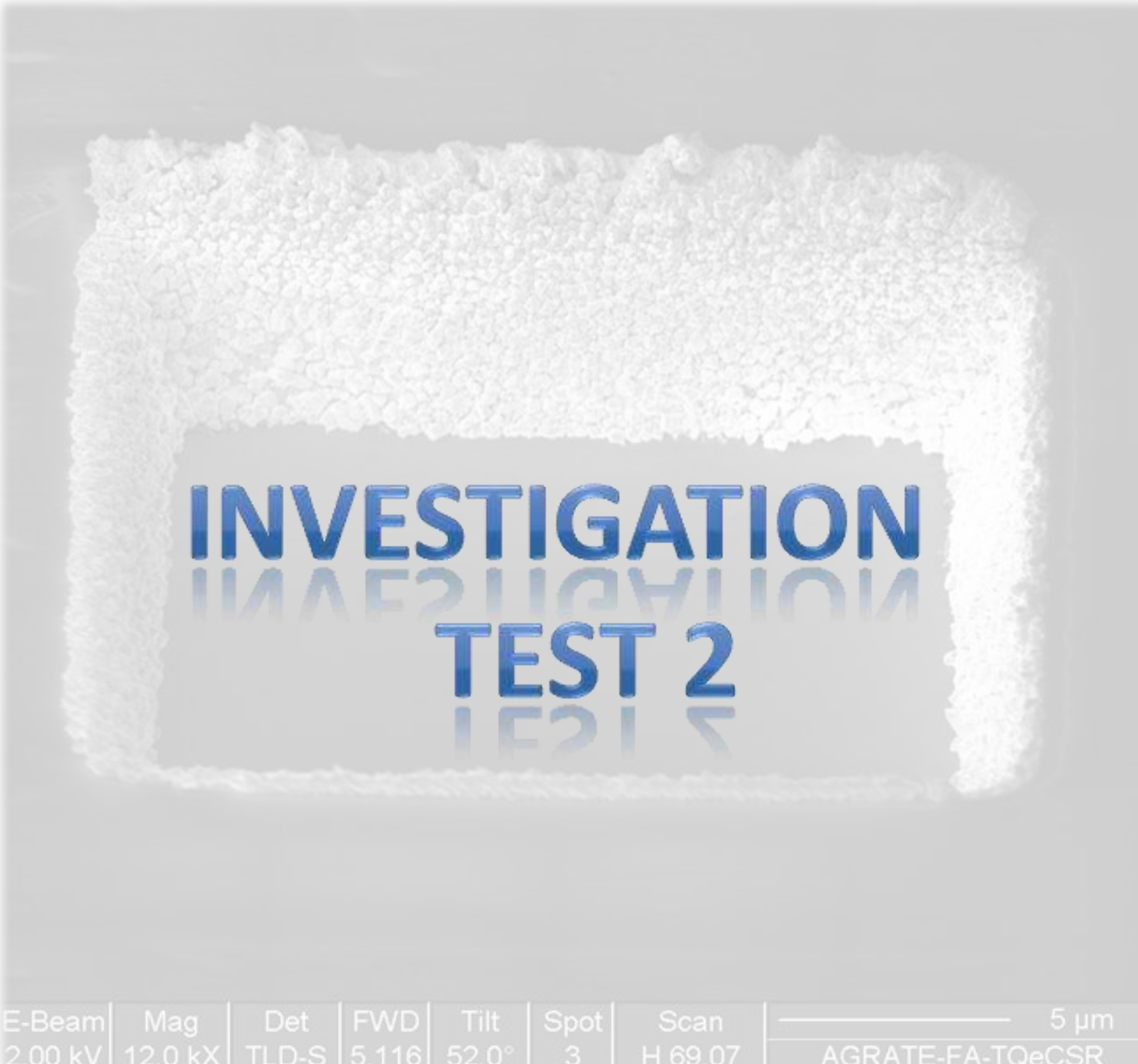


TIME	
10 min	45 min
BOX AREA	
Same bottom trench area	
ILD EXPOSED QUALITY	
Same flatness & warpness	
Same ILD over etch	
BOX OVERETCH	
~1,50µm	~500 nm





INVESTIGATION TEST 2



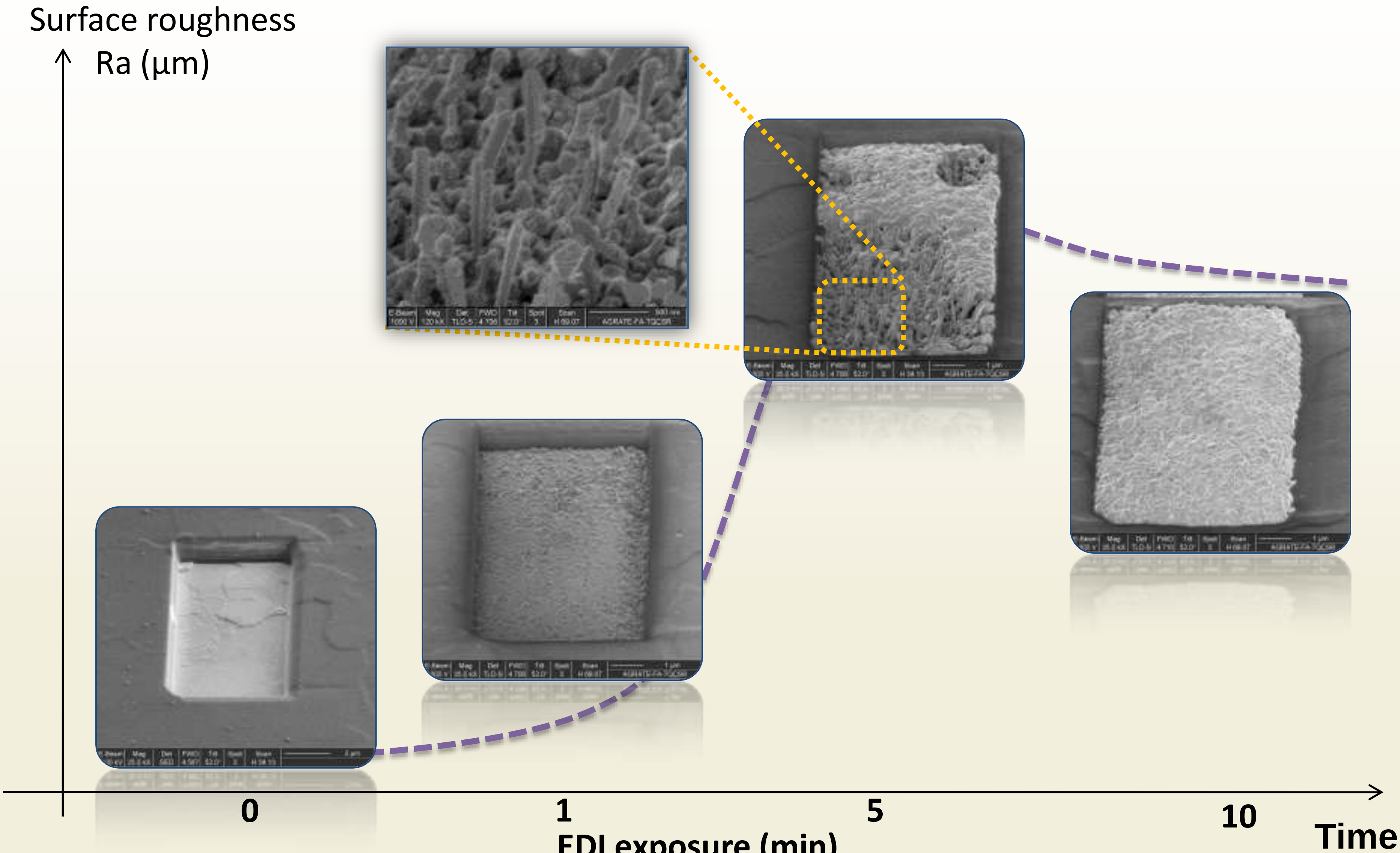
TEST 2: CONTAMINATION & CORROSION EVALUATION

What will happen during the CE to other exposed Cu areas?

EDI corrodes exposed Cu, even in areas out of FIB image field of view.

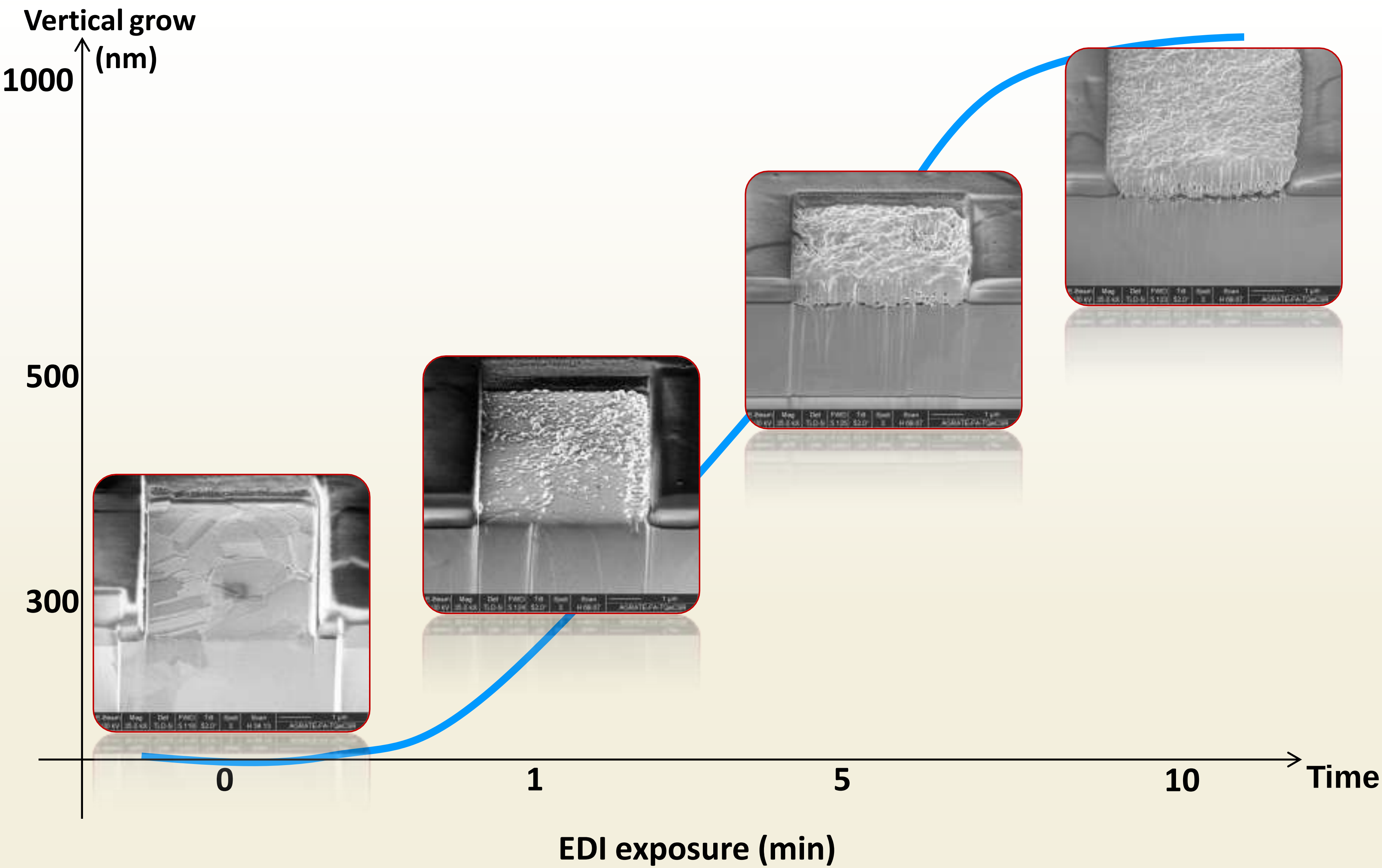
- **Goals**
  - Define over the time the Cu corrosion by exposing it to an halogen compound (here EDI)
  - Analyze parameters such as: Top surface, Corrosion & contamination progress, Artifacts
  - Measure the impact of the corrosion during the CE process and also over the time.
    - The device with contaminated area has been kept under vacuum (2.5×10^{-7} Torr) for 10 days, in order to reduce external environment contamination.
- **Setup**
  - Expose 4 areas to the gas flow, respectively 0,1,5,10 minutes
  - During the gas flow no beam rastering is applied
  - Perform cross-section and SEM analysis
  - Evaluate the contamination and corrosion amplitude in both lateral and vertical axis

TEST 2: -DAY 0- CU ROUGHNESS VS EDI EXPOSURE



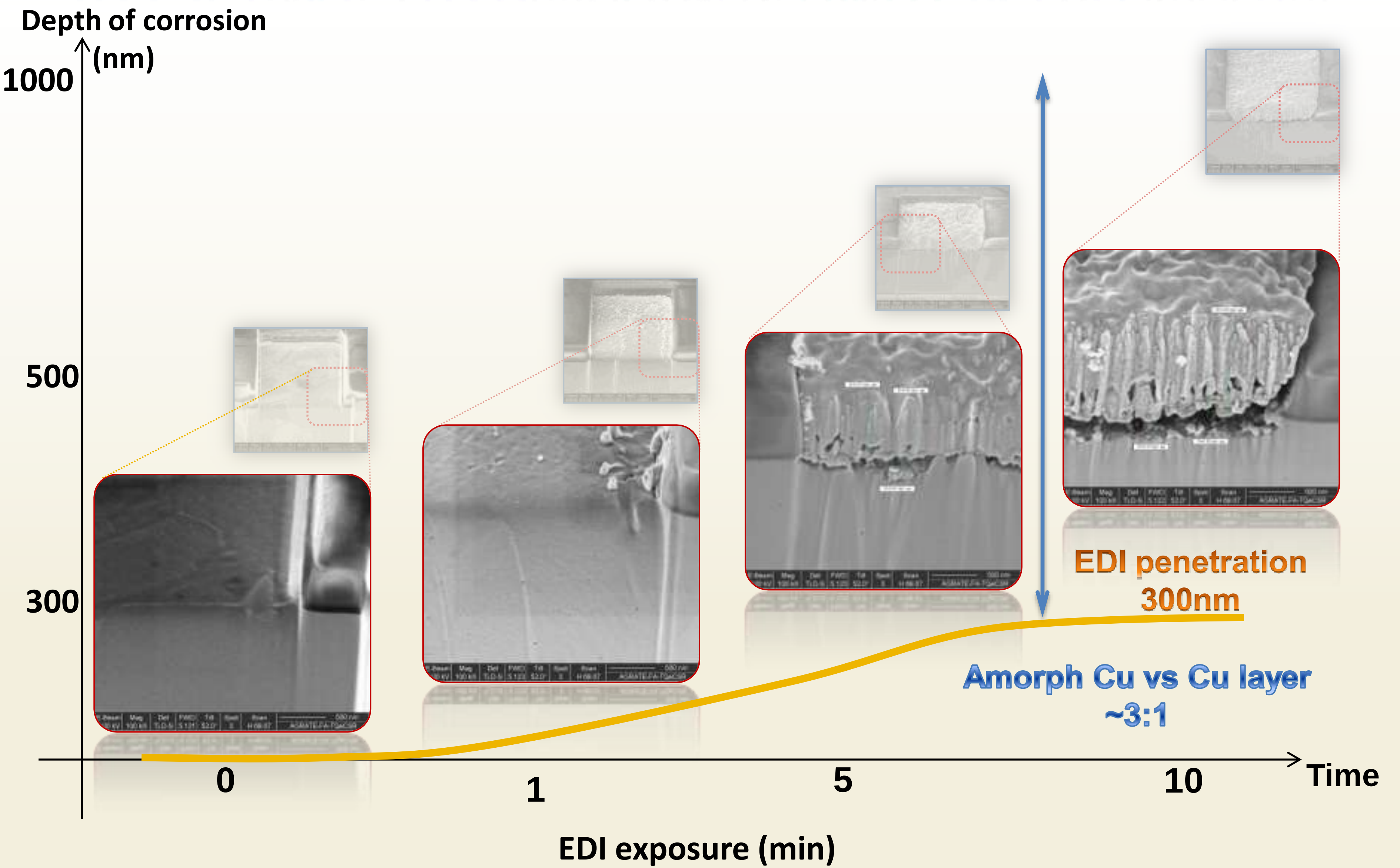
Qualitative graph

TEST 2: -DAY 0- CU AMORPHIZATION VS EDI EXPOSURE



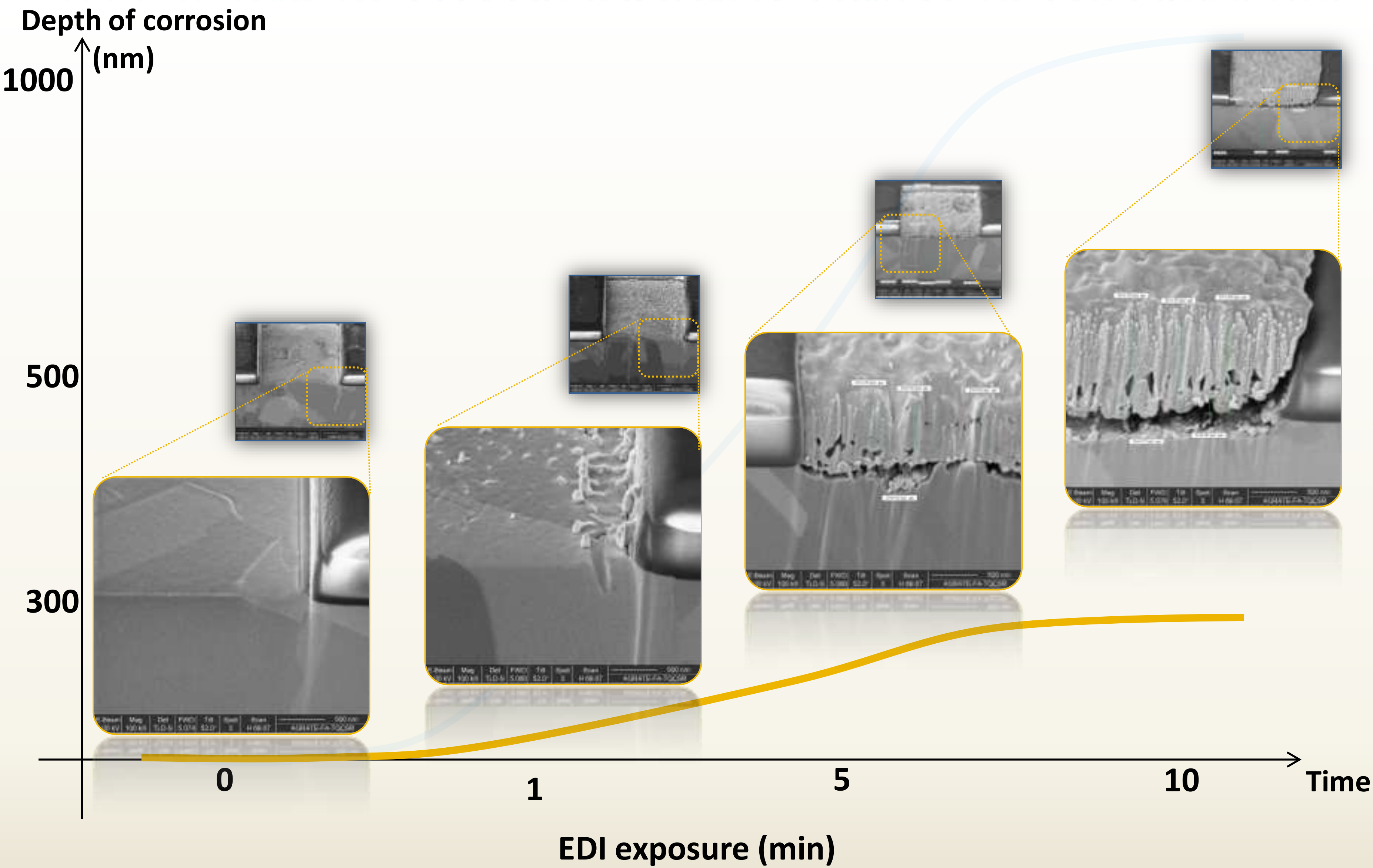
Qualitative graph

TEST 2: -DAY 0- CU CORROSION DEEPNESS VS EDI EXPOSURE



Qualitative graph

TEST 2: -DAY 10- CU CORROSION DEEPNESS VS EDI EXPOSURE



Qualitative graph

CONCLUSION

- **Bulk-EDI RECIPE**
  - The empirical results presented above qualify the very fast & planar Cu power plane etch rate
  - The recipe is useful for large and thick Cu plane and is 4 time faster than Cu-II recipe.
  - Turning strong crystallographic material in an amorphous one helps to enhance sputter yield.
  - Works better if in presence of underlying thick dielectric
  - The benefit of reducing the time to remove Cu power plane is surely an advantage for CE throughput
  - Before introducing EDI into the FIB chamber for a Cu device edit, user must make sure all other exposed Cu areas are covered or it will be corroded as shown above. On thick metallization it is not an issue.

Acknowledge

– CAPITANIO Emanuele *STMicroelectronics*
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References

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