

DCG Systems

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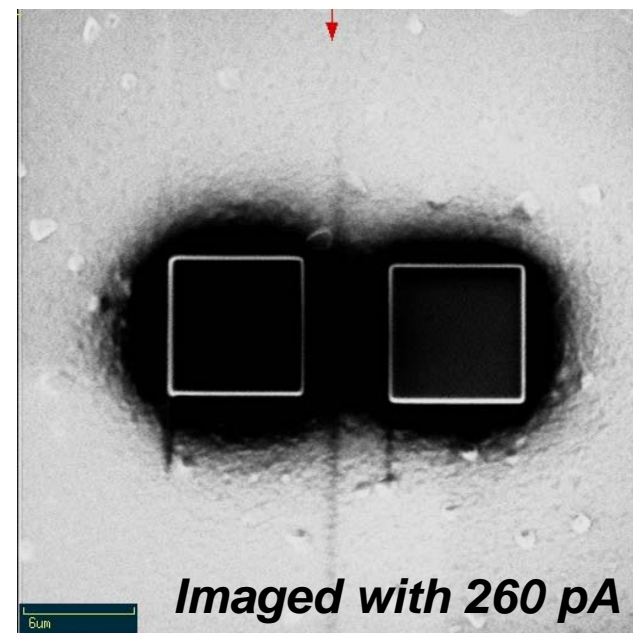
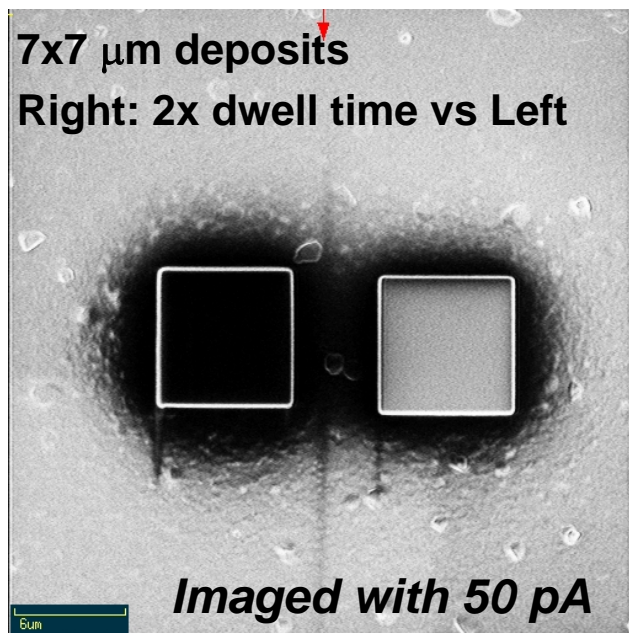
EFUG 2008 Maastricht, the Netherlands

Higher Resistivity Dielectric

VV Makarov, T Malik, R Jain, T Lundquist

Deposition Quality Control

- Insulator deposition quality controlled by beam scanning speed
 - Higher scan speed → better insulator quality
- Deposited insulator darkness: a quality check
 - Insulator “Darkness” depends on imaging current
 - Higher the current density → the darker the insulator image



- All quality checks were performed with same 50 pA
 - Exceptions: depositions using low currents: 3 & 10 pA
 - Deposition current used but with higher magnification to maintain average current density

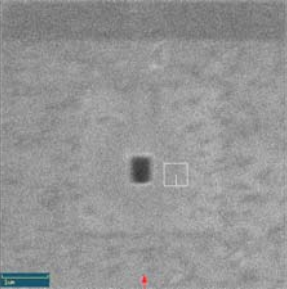
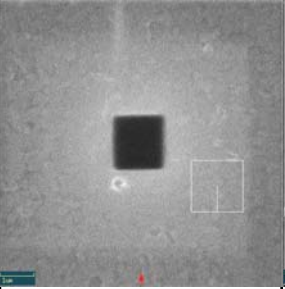
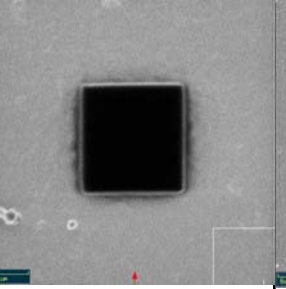
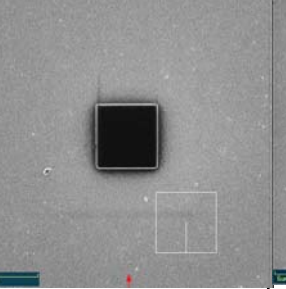
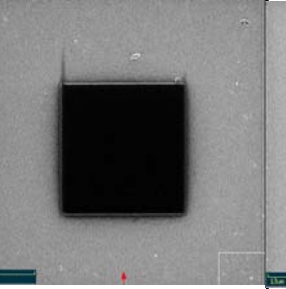
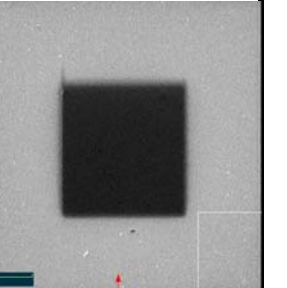
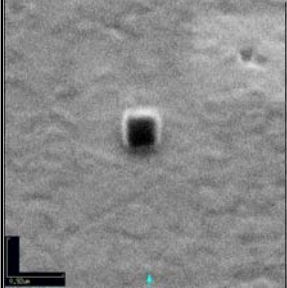
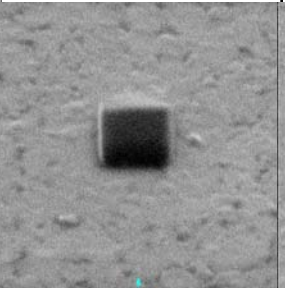
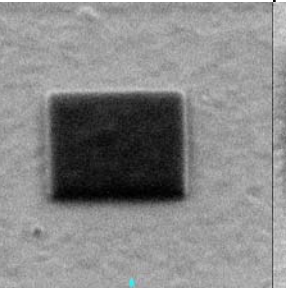
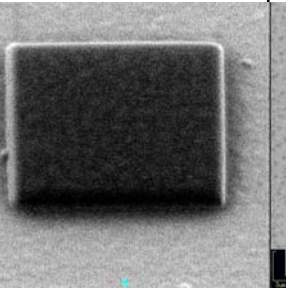
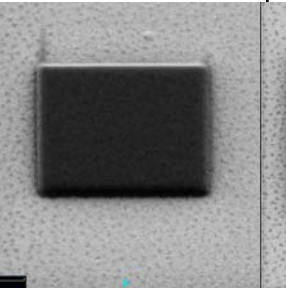
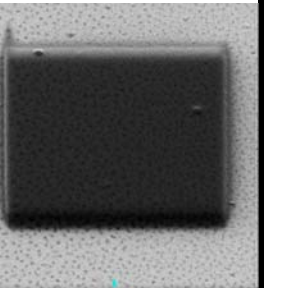
Deposition Stability

- For process stability, precursor surface accumulation rate is important.
 - Each frame should start no earlier than when precursor quantity saturates
 - Precursor accumulation rate \propto “residence time”
 - ◆ Average time a molecule sits on the surface before leaving
 - ◆ Function of precursor vapor pressure.
 - Residence time estimated from vapor pressure
 - Accordingly, refresh time = frame time

Optimized deposition conditions

- Insulator deposited: smooth & without gaps/spaces
 - Pixel & line overlap important
 - Dwell time $t: \leq 100$ ns, for continuous beam scanning
 - Single line deposition width confirmed experimentally for each current
- Precursor Pressure low 10^{-5} Torr;

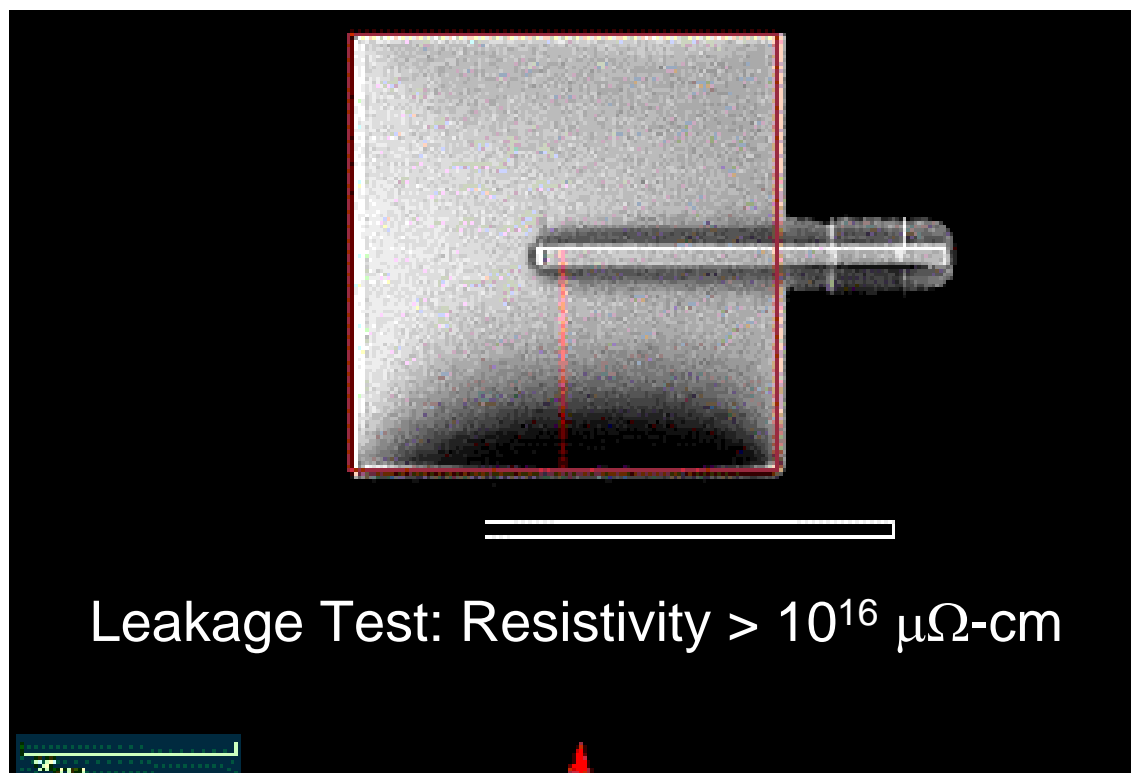
Depositions

Beam Current	3 pA 0.5 x 0.5 μm	10 pA 1.5 x 1.5 μm	50 pA 3 x 3 μm	260 pA 7 x 7 μm	1000 pA 15 x 15 μm	4000 pA 30 x 30 μm
Plan view						
Tilted view						

Insulator Deposition test structure

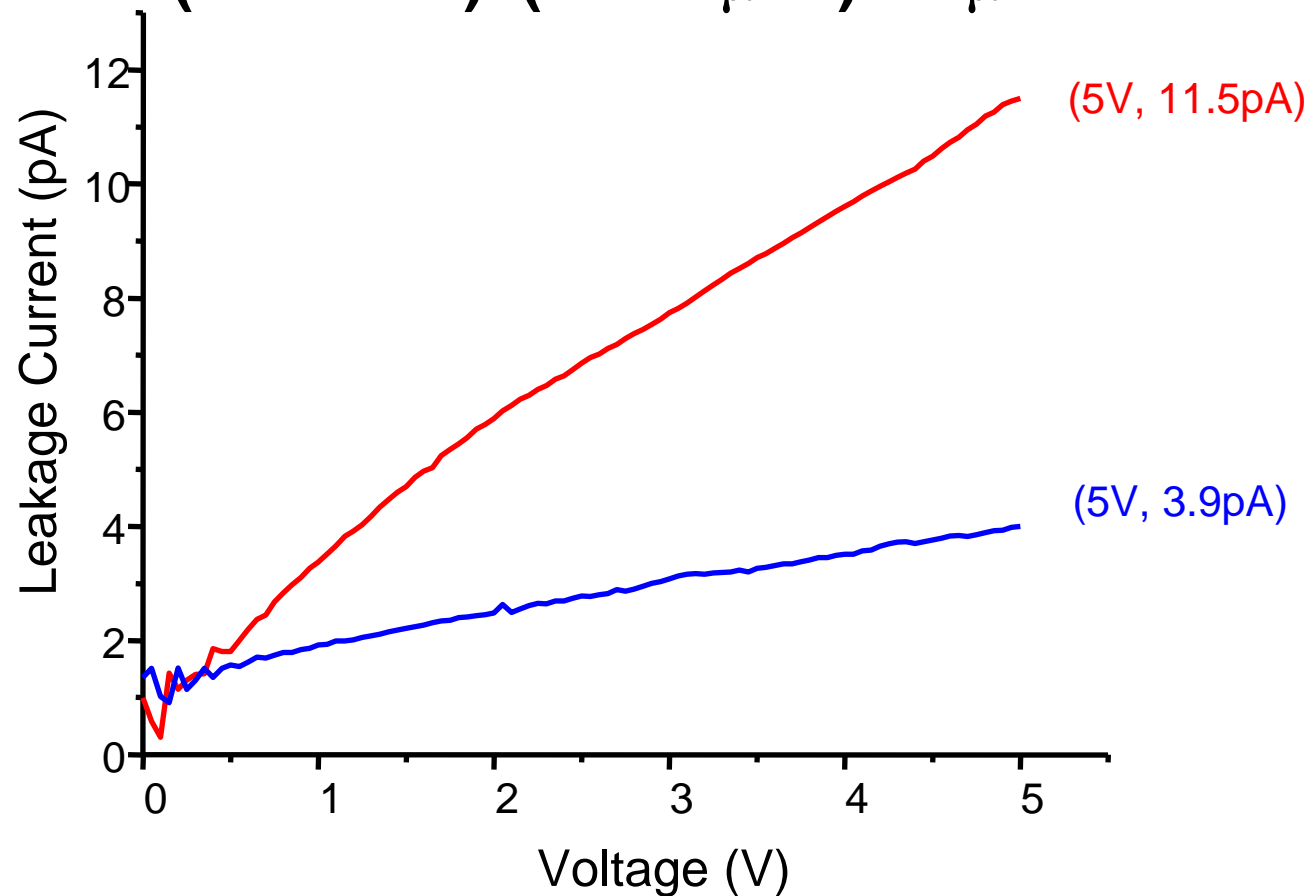
Protocol

- | | | | |
|----|------------------|--------------|-------------------------------|
| 1. | XeF ₂ | 50 x 50 μm | to expose Al power plane, |
| 2. | Ins Dep | 49 x 49 μm | ~0.5 μm thick |
| 3. | Ins Dep | 52 x 52 μm | ~1.0 μm thick |
| 4. | XeF ₂ | 1.5 x 1.5 μm | to expose Al trace |
| 5. | Moly Dep | 1.4 x 1.4 μm | for via to Al trace |
| 6. | Moly Dep | 50 x 50 μm | to form contact pad |
| 7. | Moly Dep | 50 x 2 μm | to connect contact pad to via |



Results

- Vertical leakage current
- Leakage current between two pins (on same chip) NOT connected by an insulator deposition structure
- $R = 5V / (11.5 - 3.9) \times (50 \times 50 \mu\text{m}^2) / 1.5 \mu\text{m} = 1.1 \times 10^{16} \mu\Omega\text{-cm}$



Summary

- Single component Precursor
- High resistivity $> 10^{16} \mu\Omega\text{-cm}$
- Yield = 1 to 3.5 $\mu\text{m}^3/\text{nC}$
- Rate = ~60 nm/min