New FA Opportunities with Ultra Thin Silicon

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Outline

- FIB Backside Preparation Procedure
- CtS for Probing & FET Characterization
- E-Beam Probing from chip backside
- Backscattered Electron Microscopy
- Outlook

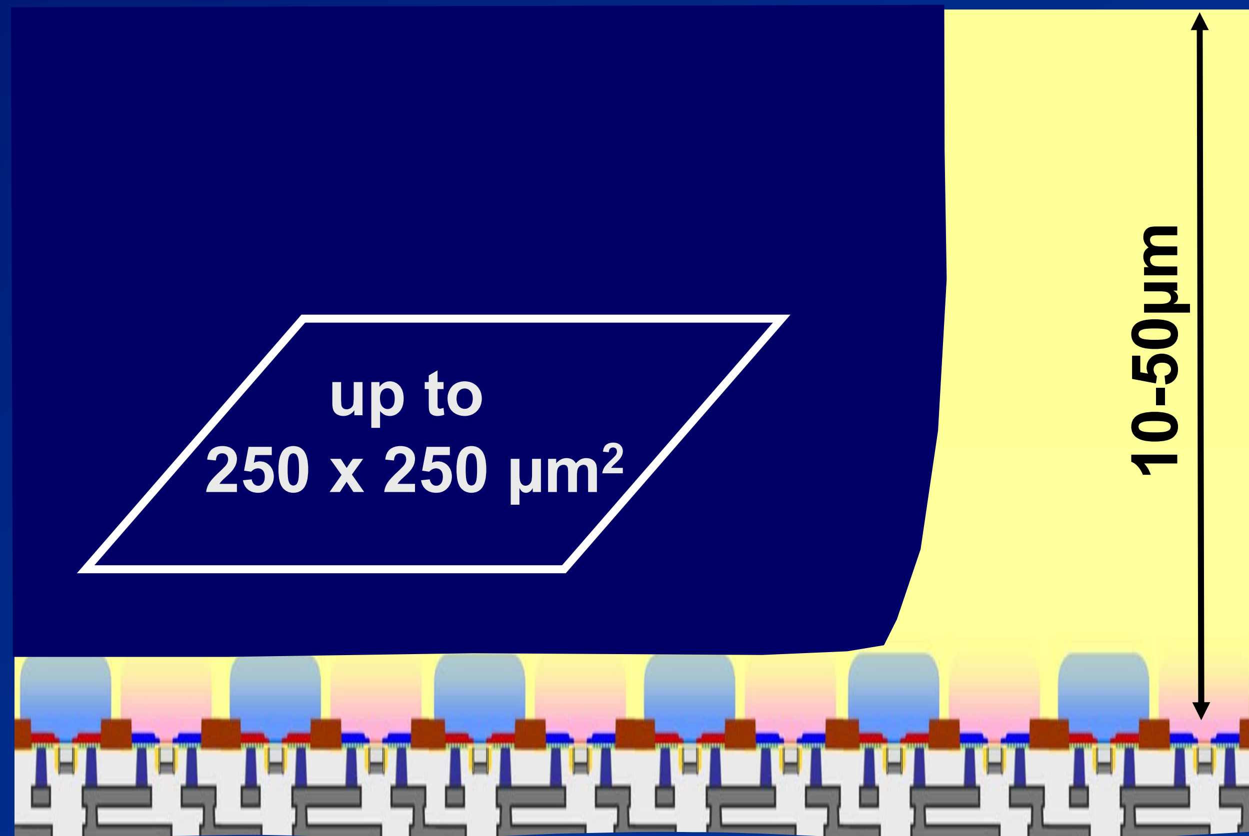
FIB Backside Circuit Edit Procedure

- mechanical thinning
- localized FIB trench
  - stopping on n-wells

trench placement

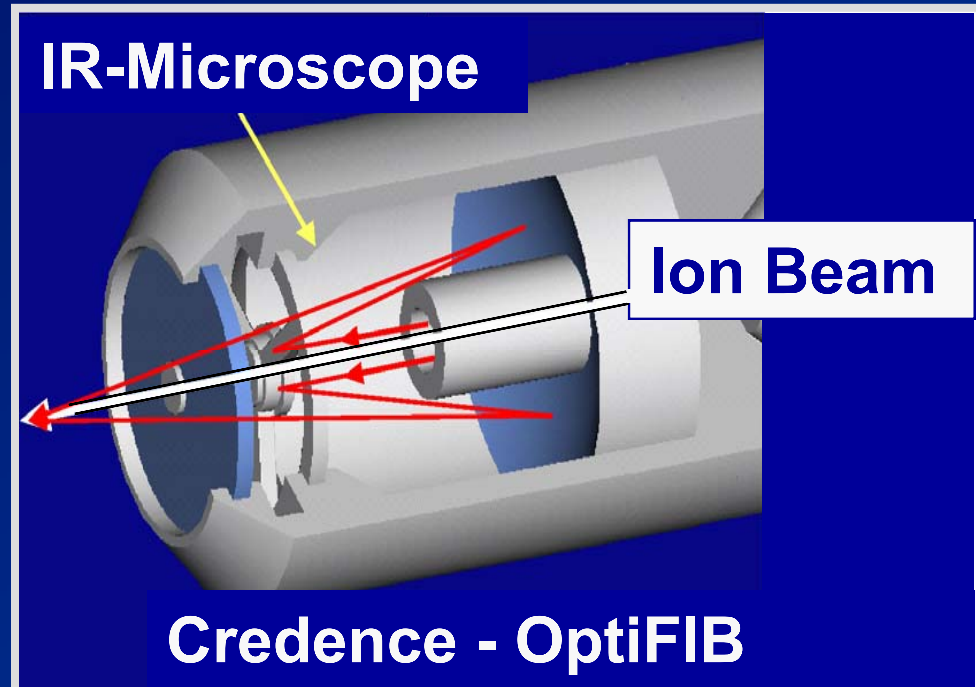
?

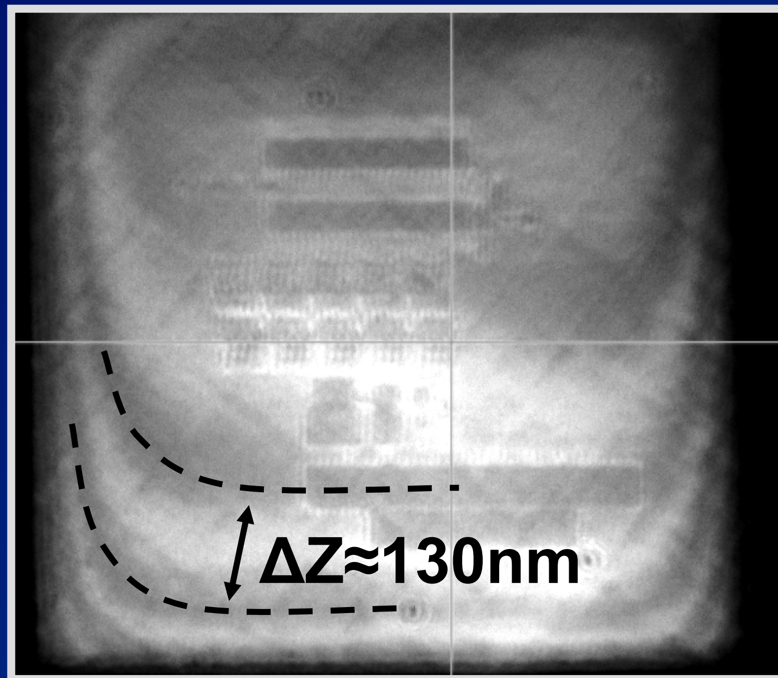
planarity control



Navigation & Planarity

Global navigation through silicon with co-axial IR and ion column



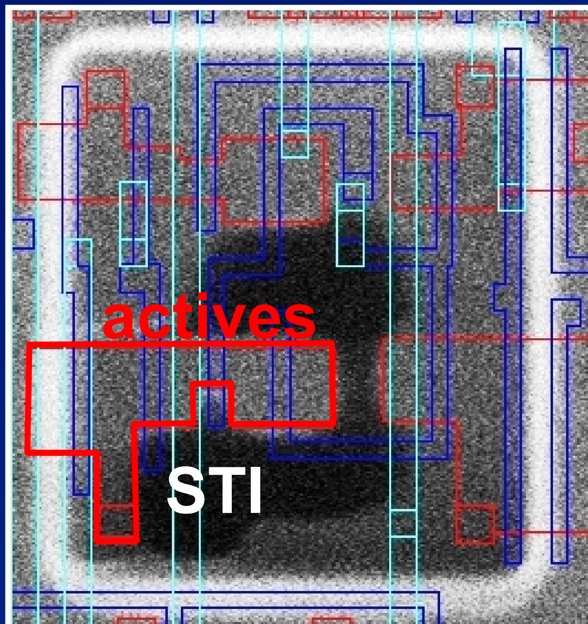


Co-planarity check of trench bottom to chip levels with interference rings (fringes)

FIB Backside Circuit Edit Procedure

- mechanical thinning
- localized FIB trench
  - stopping on n-wells
  - stopping on STI

    < 400nm remaining Si
- local alignment

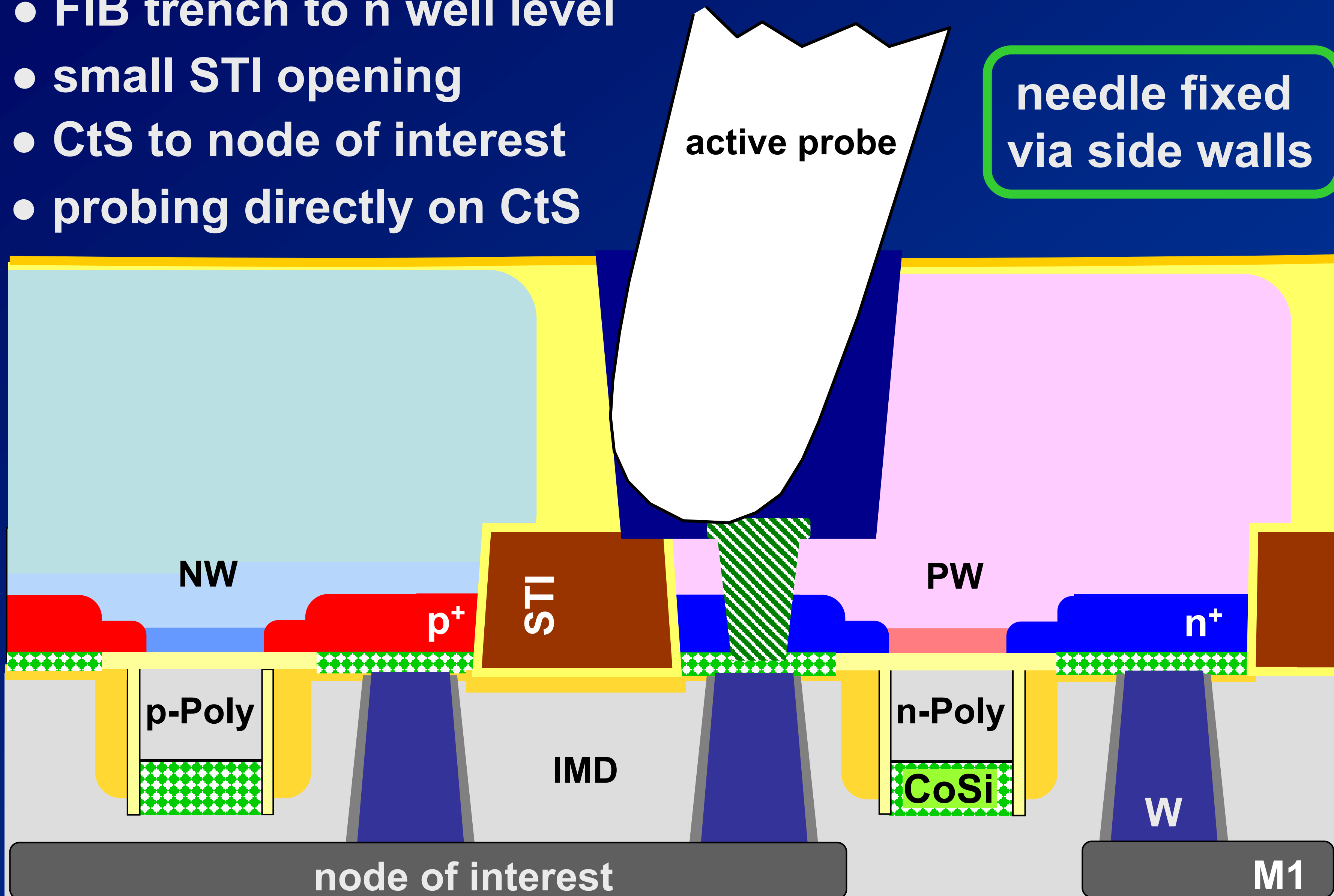


Ultra Thin Silicon

4 - 40000µm²

STI

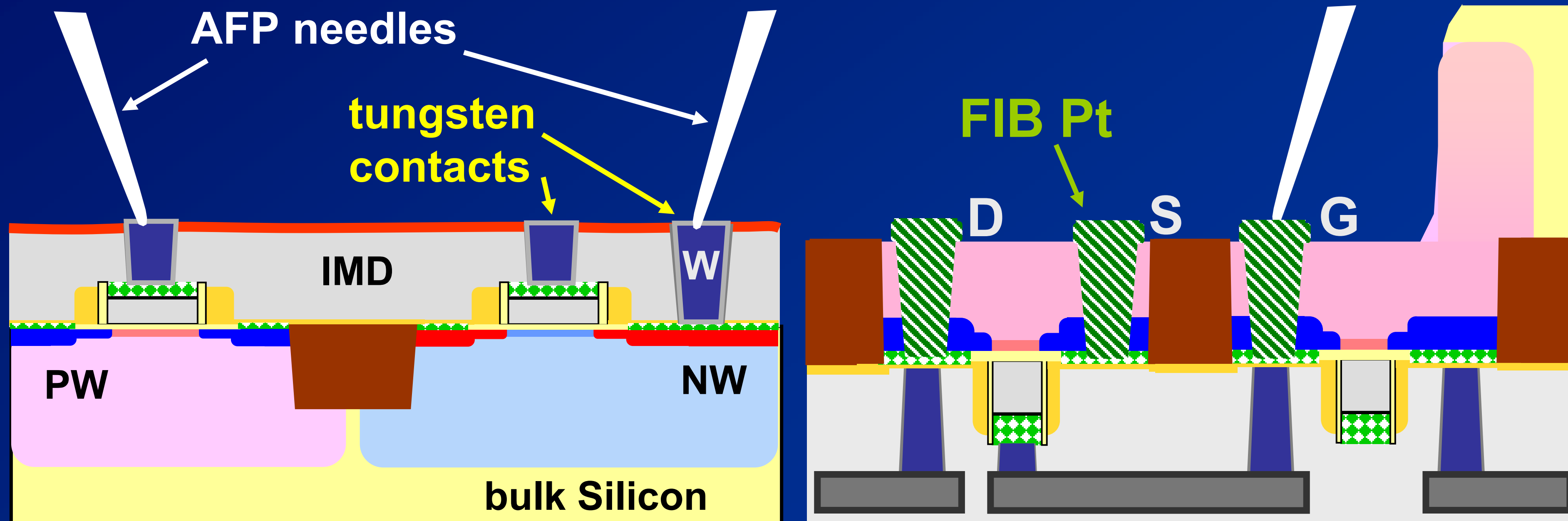
Application of CtS for Backside Probing



frontside AFP backside

- parallel lapping down to contact layer
- isolated devices
- low ohmic contact
- DuT disfunctional

- FIB backside process
- devices not isolated
- creation of new circuit nodes
- DuT functional

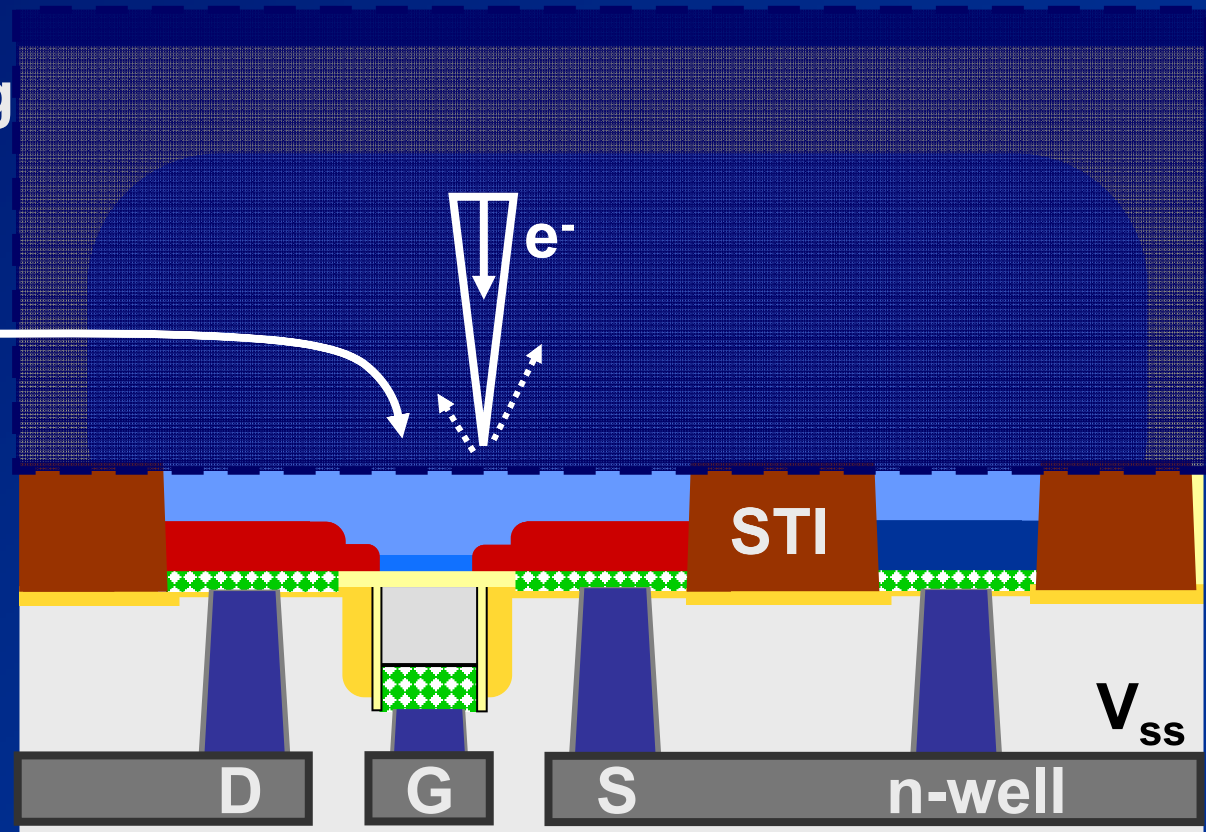


Accepted publication in ISTFA 07

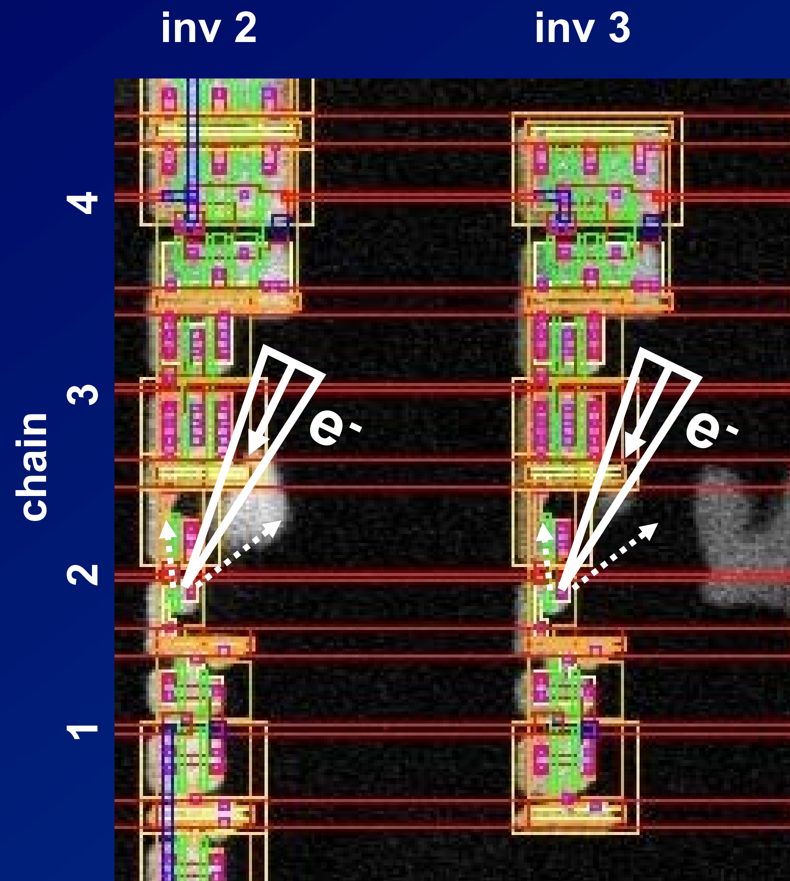
FIB Created SOI Devices

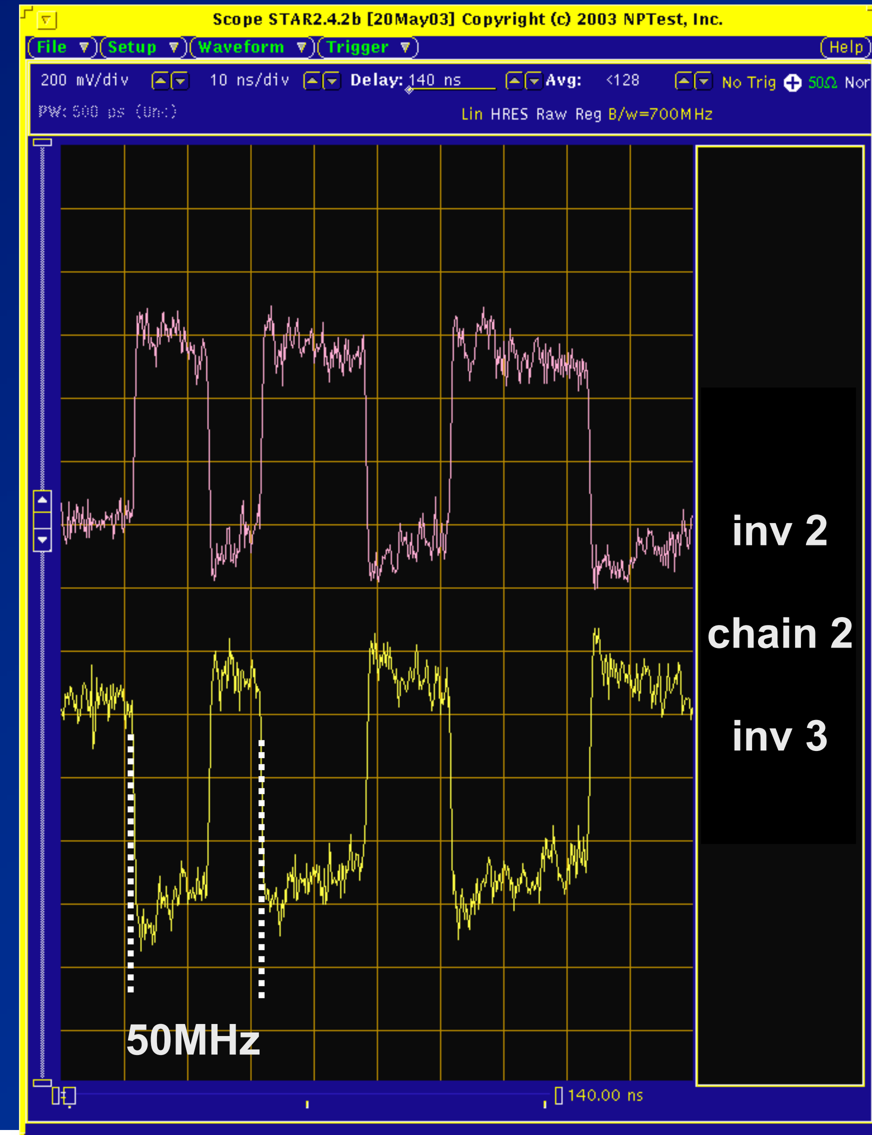
- trench to n-well does not alter device physics
- trench to STI level
  - well / bulk disconnected
  - similar to PD SOI
  - FET body floating

body potential is modulated by any switching of the device



Backside E-Beam Probing



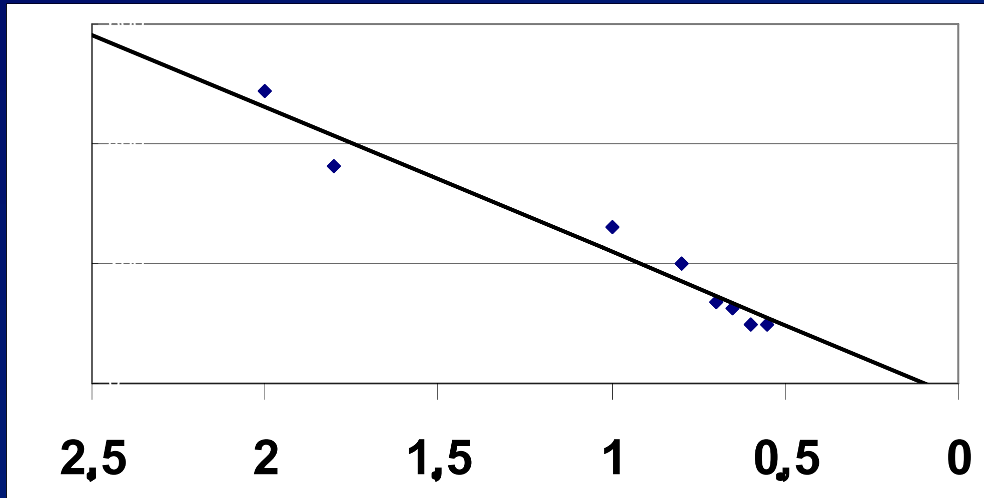


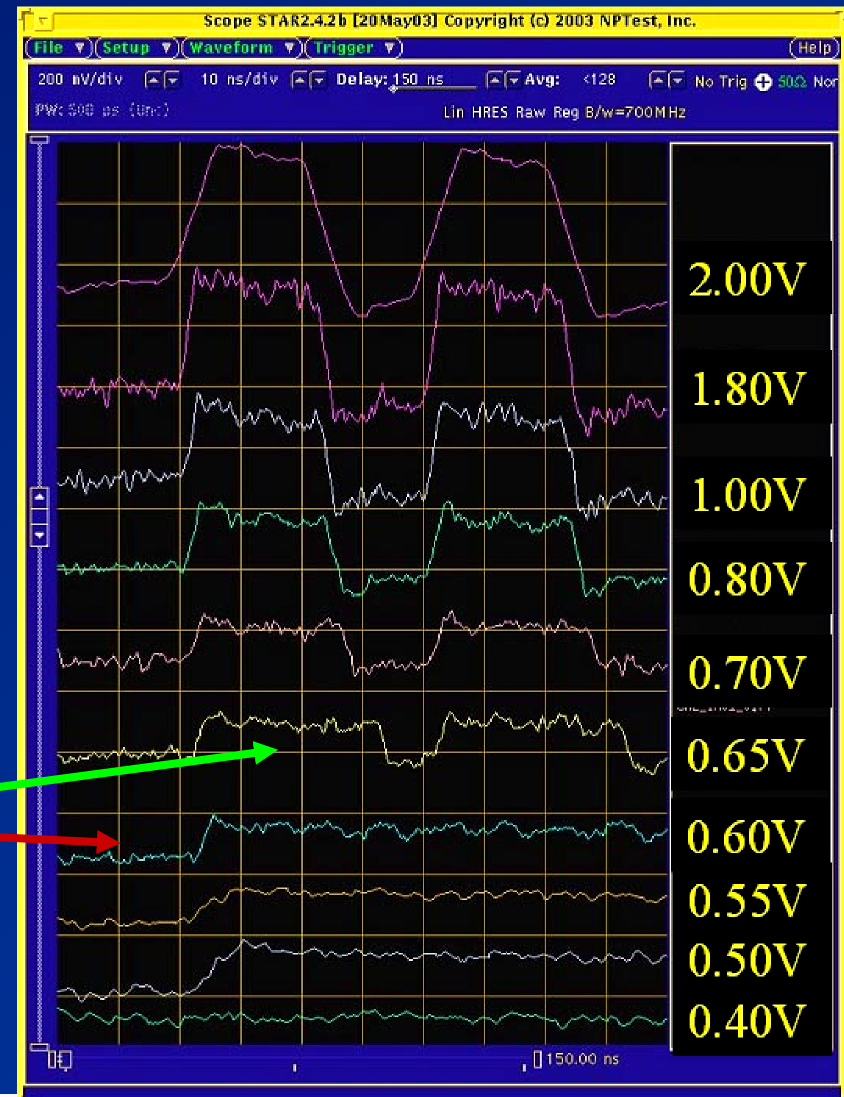
Accurate Data Monitoring

Very good SNR

Voltage Scaling

Linear Voltage Dependency



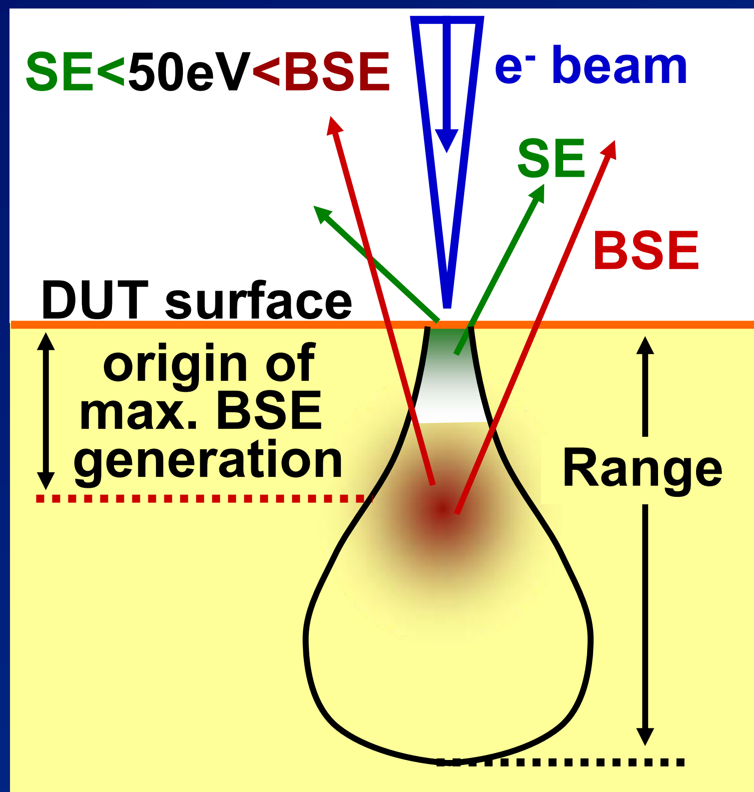


Transition from Pass to Fail

Backscattered Electron Generation

- e^- range is beam energy dependent
- surface information with SE < 50eV
- BSE are generated in sample volume

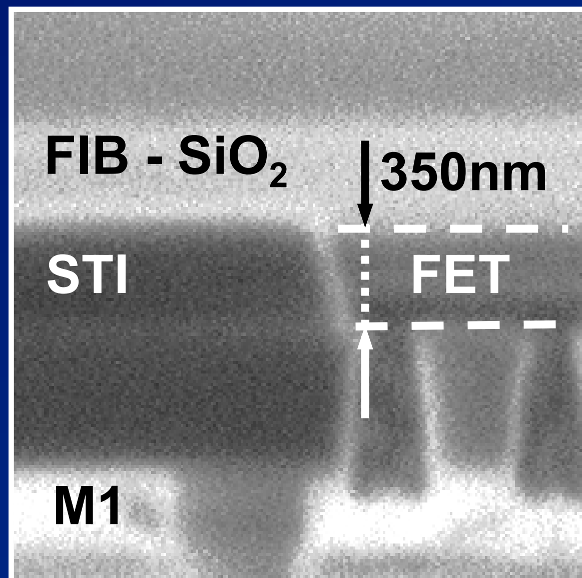
  ➔ depth of max. BSE generation = $f_{(\text{beam energy})}$

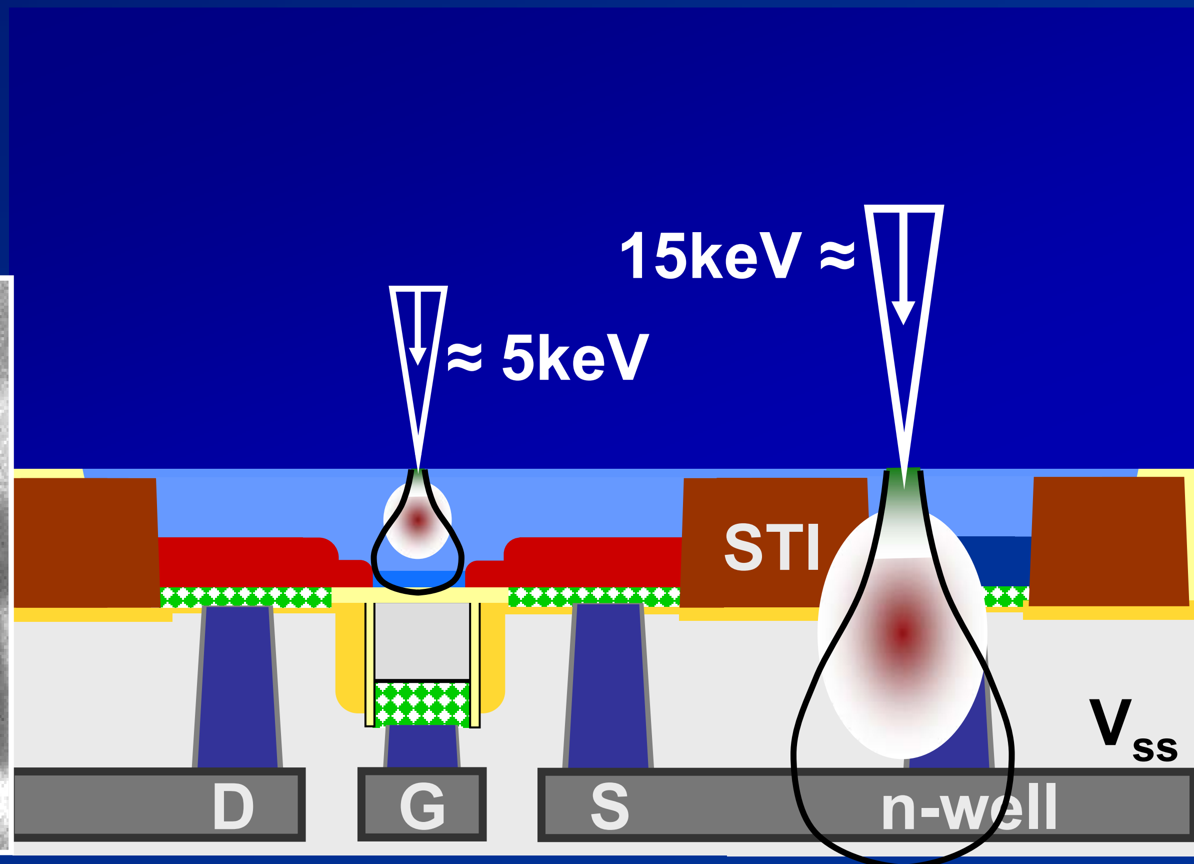


Beam Energy [keV]	SiO_2	
	Range [µm]	max. BSE [µm]
1	0.03	~0.007
5	0.45	0.092
10	1.55	0.31
15	3.22	0.73
20	5.31	1.25
30	11.32	2.32

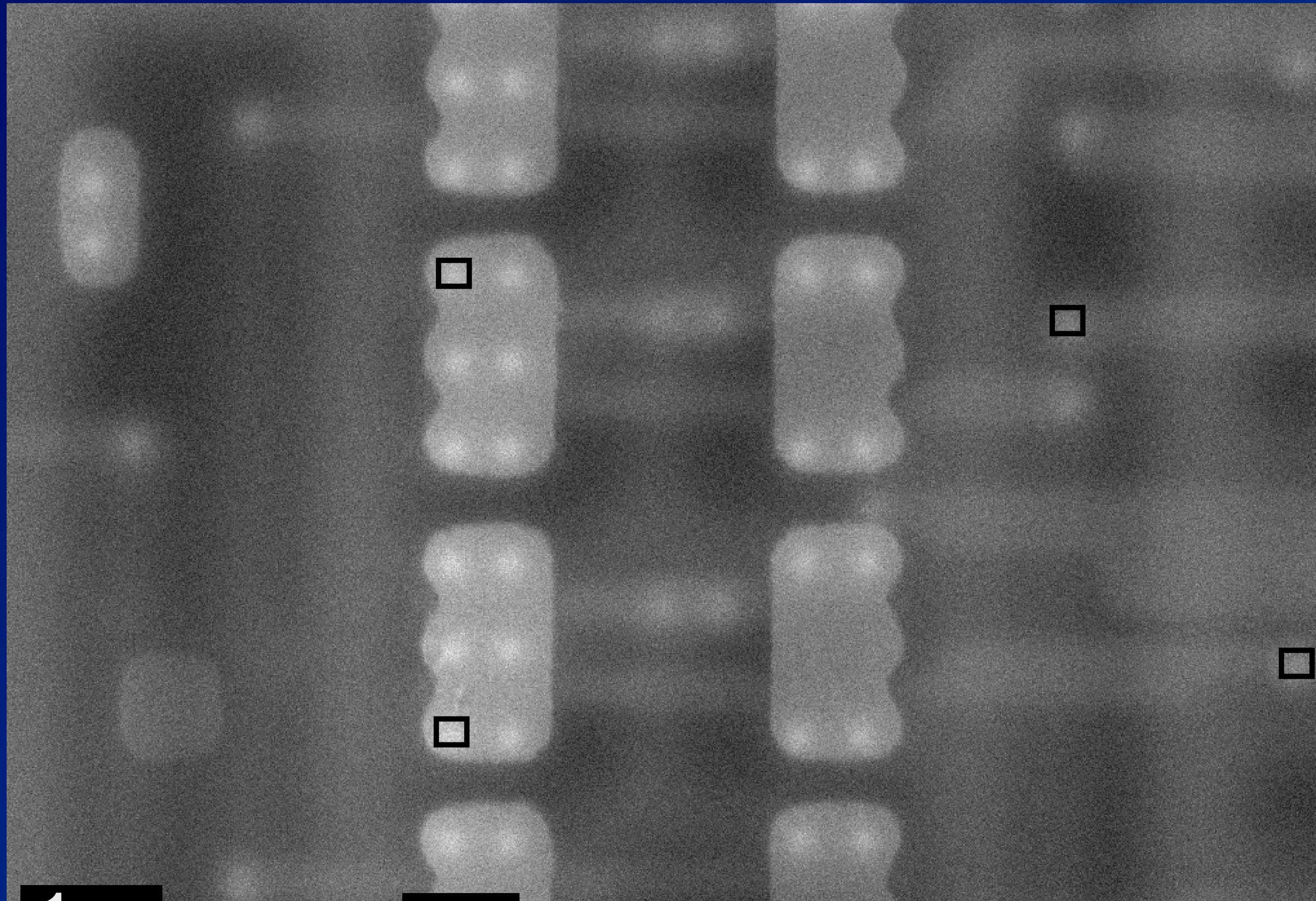
3D Chip Inspection

- remaining thickness below 400nm
- Backscattered Electron Microscopy
  - scanning through the still functioning DUT





One Image = STI, diff, poly, W….



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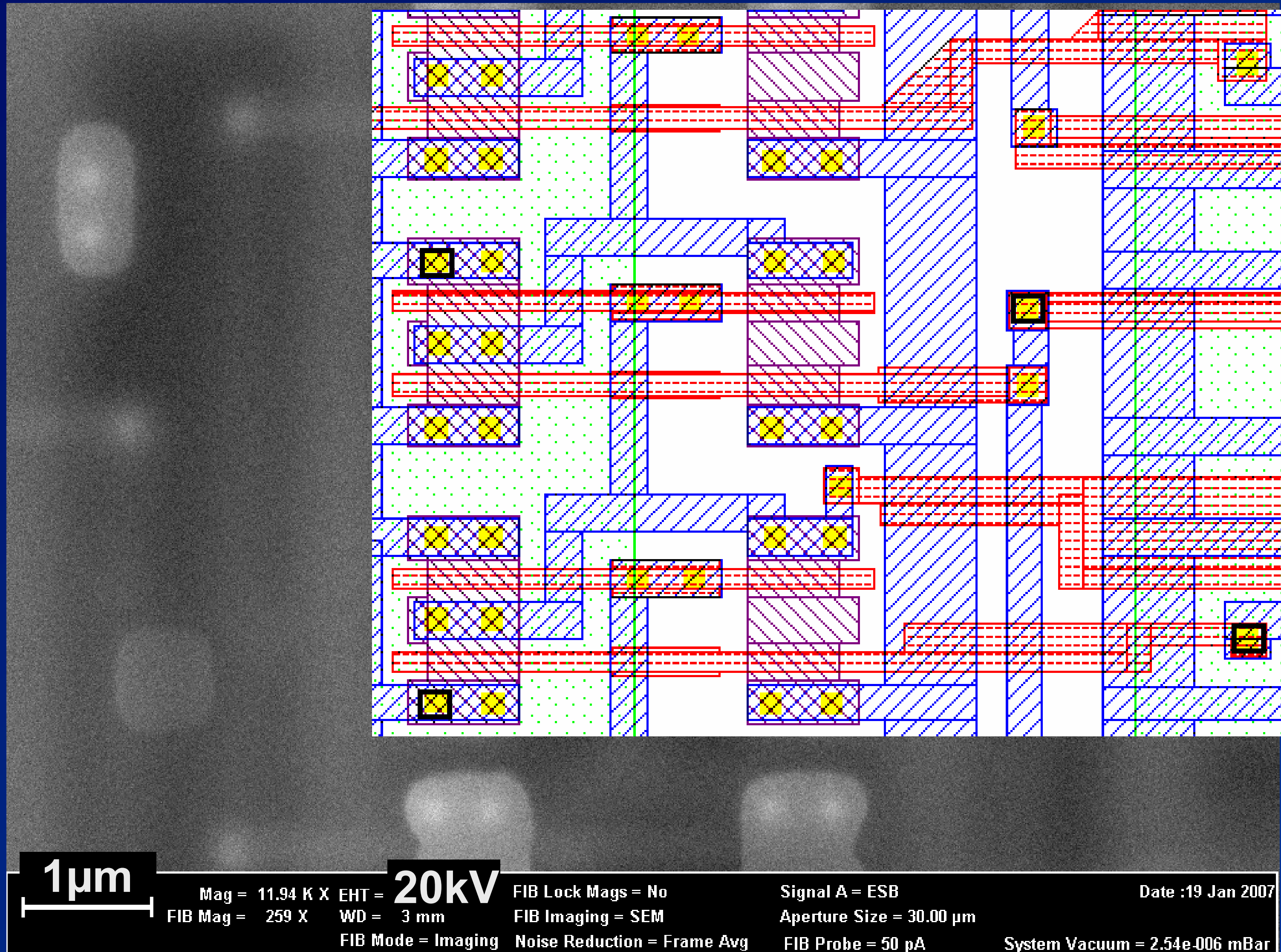

Summary

- Ultra Thin Si offers various new applications
- direct probing with reduced impact
- non destructive single FET characterization
- Backside E-Beam Probing
- non destructive 3D chip inspection
- allows complete FA through chip backside
  - no depackaging / DuT stays functional