# Through Silicon Editing

T Lundquist, M Thompson, E Le Roy and W Thompson
NPTest Probe Systems

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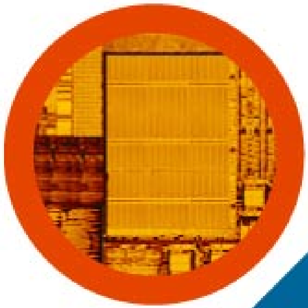
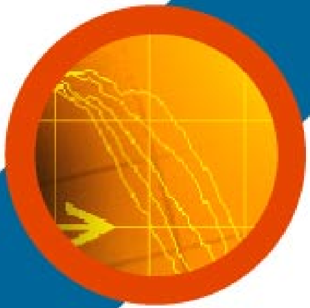
European FIB Users Group


# Purpose

- Review processes in through-silicon editing
- Review issues in through-silicon editing

# Outline

- Introduction
- Issues:
  - Device thinning,
  - Substrate isolation,
  - Reduction of active areas,
  - Leakage currents
  - Contacting active areas
- Conclusion

# Introduction

- New practices to Edit ICs through silicon
- Interconnects: passive elements
  - high isolation resistance cuts
  - low resistance contacts
  - ion beam interactions:
    - charge dumped into floating gate
    - damage evidenced by changes in transistor parameters
- Transistors: sensitive active areas
  - before interconnects reached
  - ~50% of through silicon edits involve diffusions (Intel)
  - Why
    - Accessibility of diffusions
    - Diffusion density precludes FIB operations without milling diffusions

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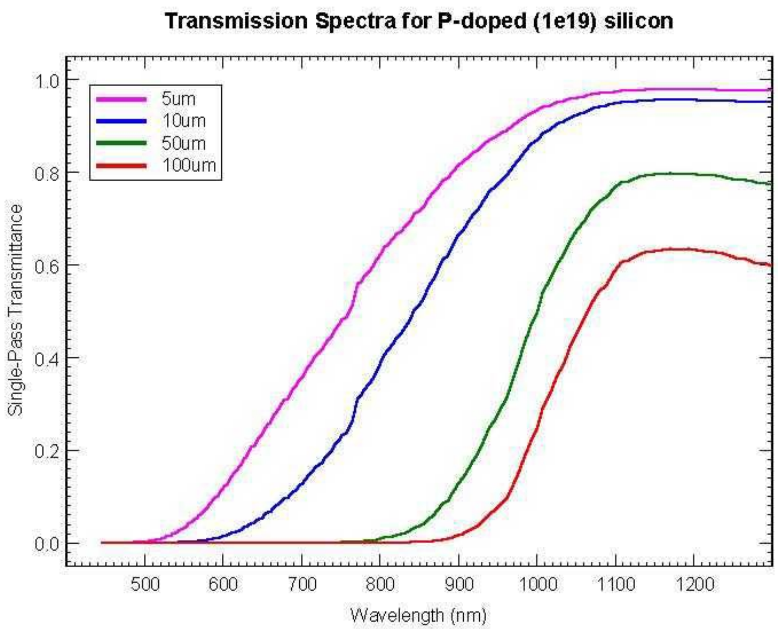
# Thin ICs before beginning an edit

- The thinner the better
  - Navigational resolution
    - Transparency > as Silicon <
  - Productivity
    - FIB operations < time consuming
- Performance unchanged
  - several frequencies and voltages
- Dies thinned, decreased reliability?
  - Package related--ceramic < plastic
  - Die size related--warpage
  - Mechanical stress
  - Early failures?
  - < 50 µm seems acceptable

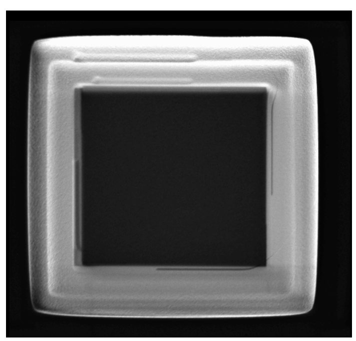


# Doped Silicon is a conductor

- Most IC substrates are doped
- Vias milled through silicon:
  - Line via with dielectric
  - Filled with conductor
  - Complication: interconnection-side
    - only when editing through power planes
- FIB insulator deposition required “all” the time

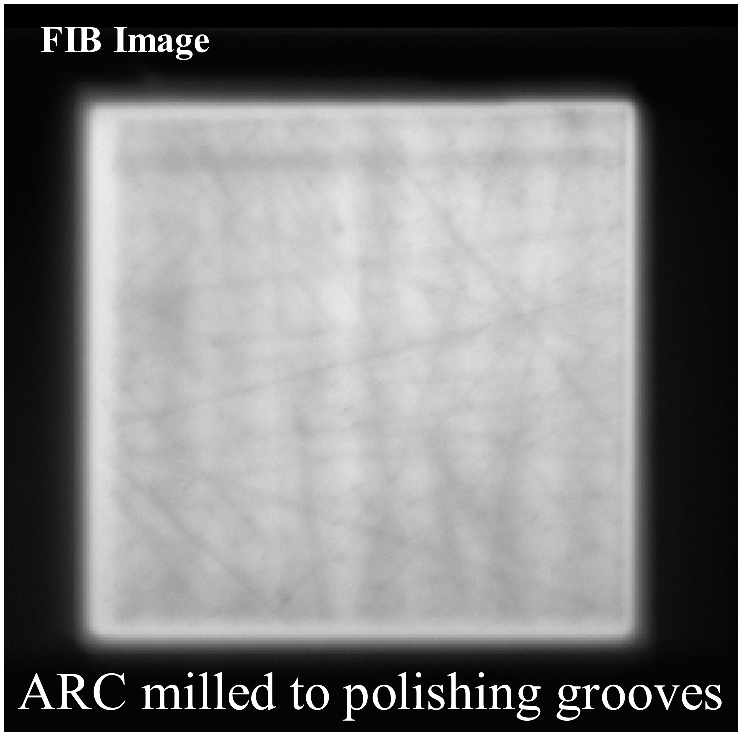
# Silicon side is not covered with dielectric

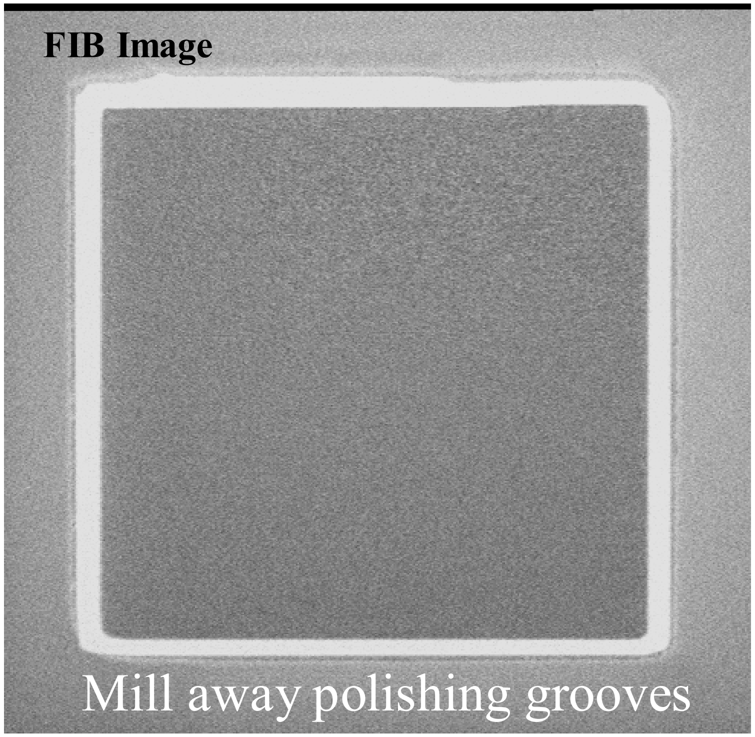
- Interconnection side covered with dielectric
  - Direct rerouting of interconnections
- Rerouting across silicon side requires dielectric
- Coating tuned to wavelength of light
  - Anti-reflective (AR) coating
    - Improves the ease of navigation--better resolution
  - Enables trace rerouting
  - Protects Si from $XeF_2$ erosion
  - Improved productivity



# ARC Removal, Surface Planarization, Trenching

- During trenching with XeF2, “pits” advance into diffusions
- Polishing grooves need to be removed

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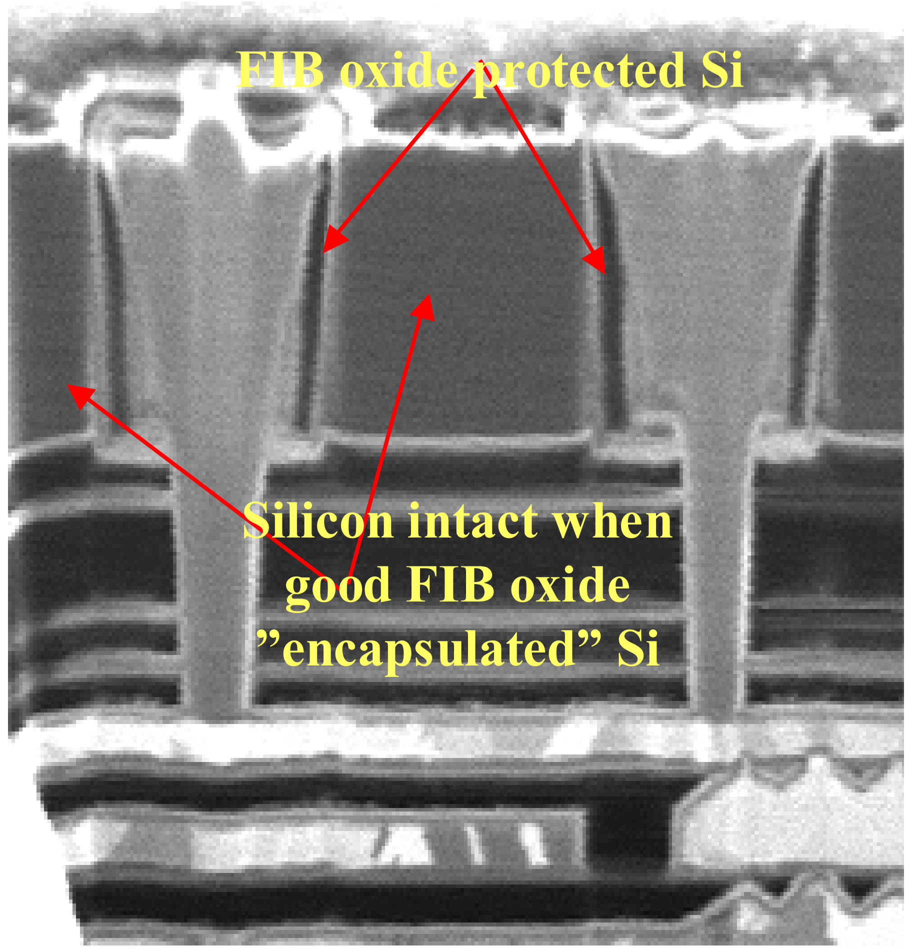
# Issue: Silicon Undercutting

Process:

- Via through silicon floor with EDI
- Fill with FIB Insulator Deposition
- Mill opening to Metal
  - XeF2 accelerates milling
  - XeF2 supports end-pointing
- Fill with FIB Conductor Deposit
- Issue:
  - Si not "encapsulated"
    - XeF2 attacks Si

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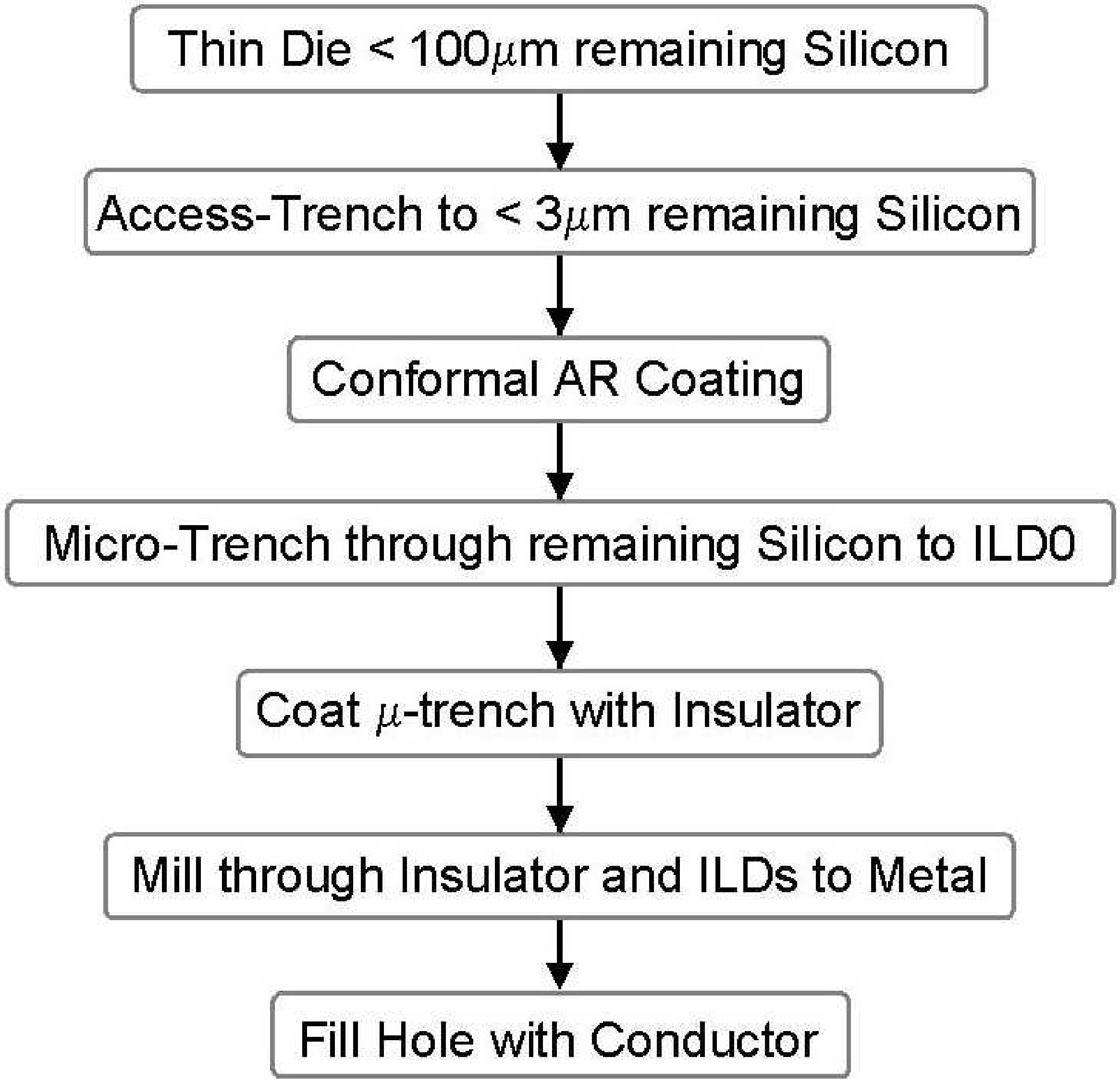
# Through Silicon Edit Flow

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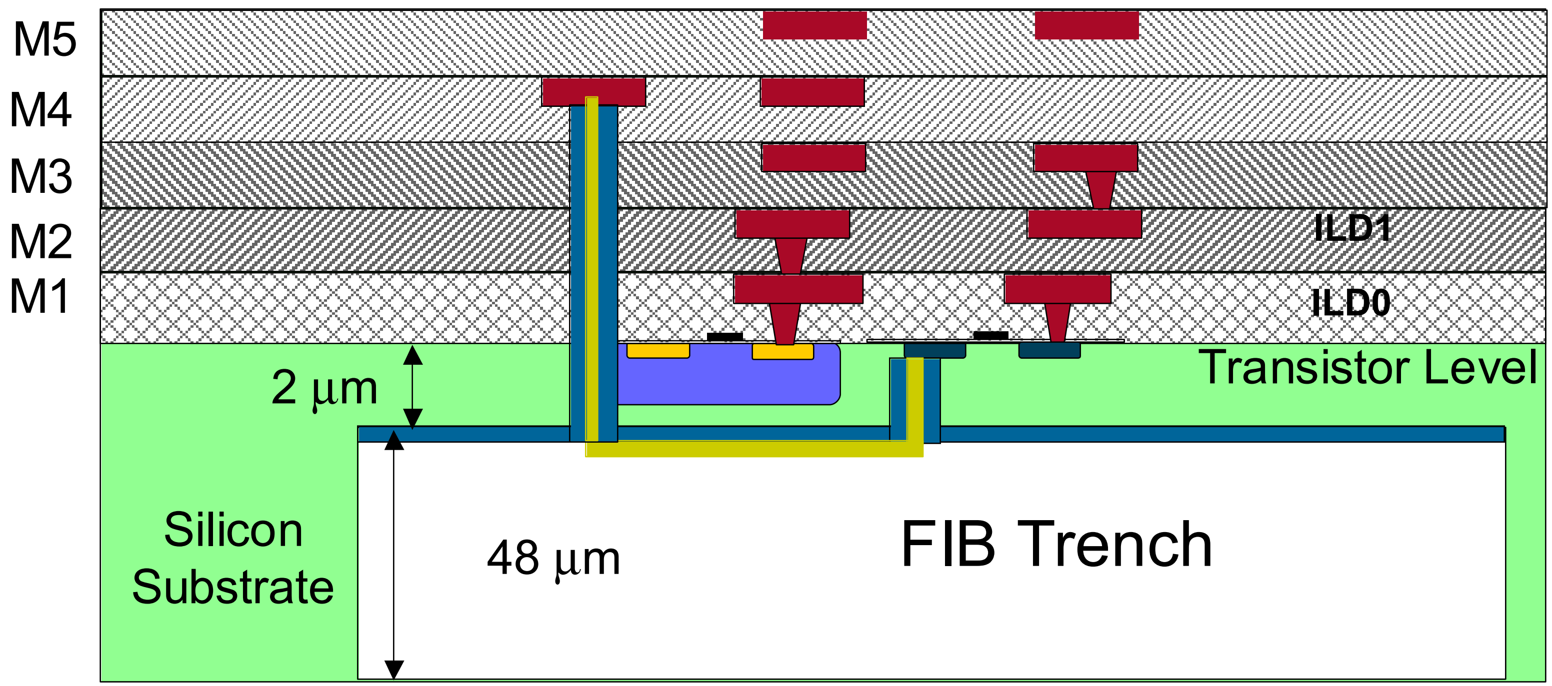
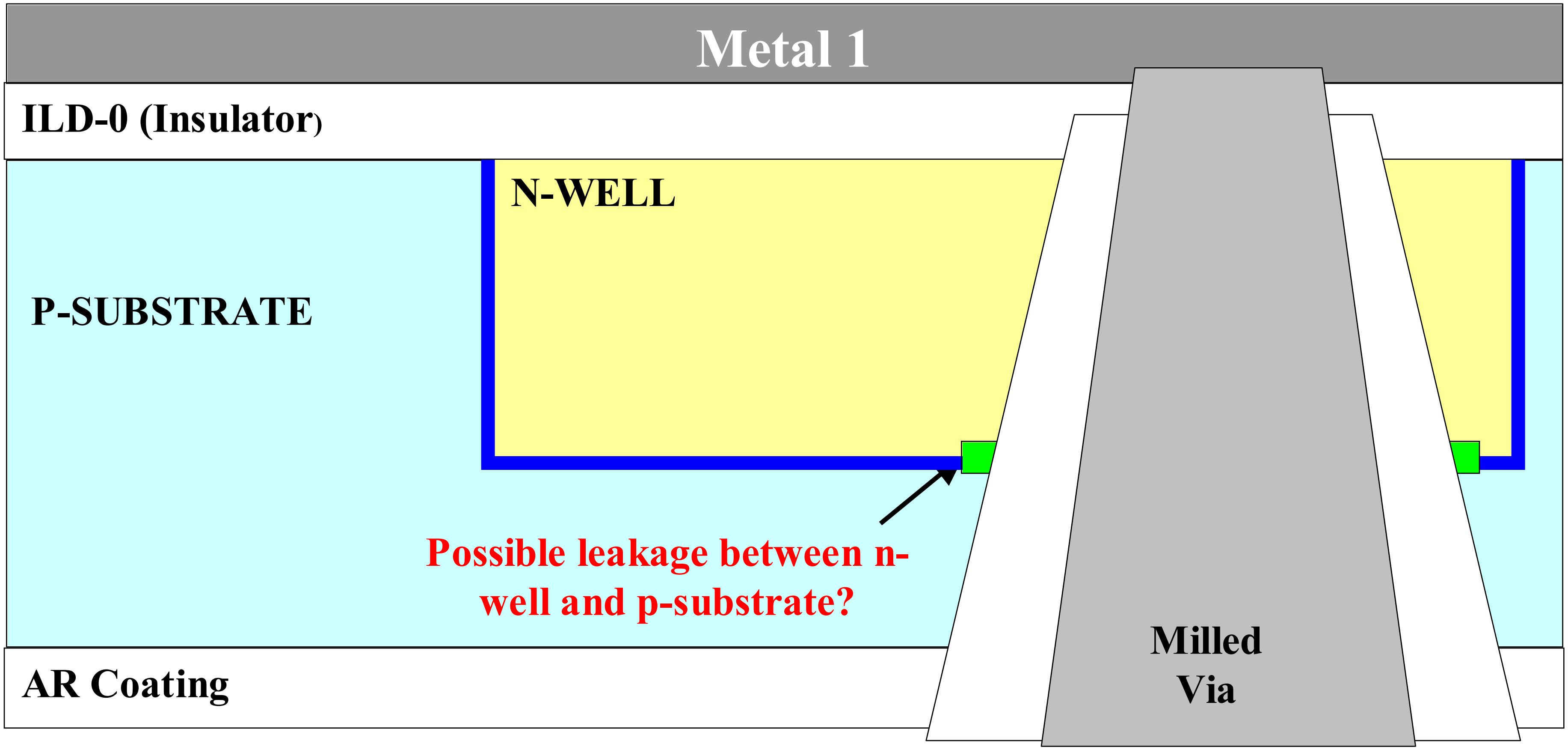
# Through-Silicon FIB Editing of ICs



# n-well size reduction

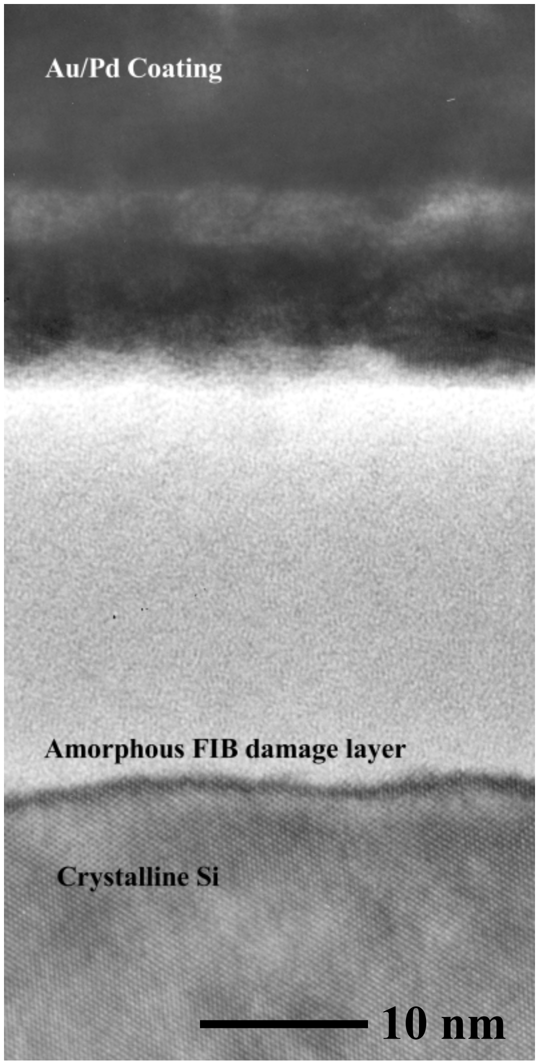
- n-well passive component to transistor structure
  - changes ought not effect transistor operation
  - leakage current?
- Transistor density increases need to trim wells
- Small reductions do not alter transistor characteristics

# Potential leakage across depletion region




Possible leakage issue from FIB damage of depletion region

# Transverse Damage to Si by 30keV $Ga^+$




From Robert Jamison, 1999

- $Ga^+$ bombardment Si (001)
- (110) damaged
  - (30keV) 24nm; (50keV) 42nm
    - Lateral straggle of ions
- Structure altered
- Composition altered

# Potential leakage across depletion region

- FIB via links p-substrate to n-well
  - Voltage difference
- Lateral damage layer by FIB (30keV) 24nm; (50keV) 42nm
- Damage layer Schottky diode type
- Gallium implanted: Depletion shifts towards back side
  - Gallium: n-dopant
- After via milled, insulator deposited before conductor
  - Interaction of insulator: Convert damage layer to insulator
- Leakage: small
  - Lee and Antoniou: 30% of one well removed
    - Device “fully functional with no detectable change in performance”
    - Photo-emission in edit area, Leakage currents?
  - Livengood et al. report leakage current increase not significant
    - Even when editing active diffusions

# Conclusion

- Metallization levels drive through silicon edits
- Editing through silicon at several companies
  - FIB dielectric is very important
    - Protects silicon
    - Isolates conductor deposition
    - Improves IR through silicon imaging
  - End-pointing very important
- Through Silicon Editing raises interesting issues
  - Leakage currents
    - Wells - substrate
    - Diffusions - wells
  - Transistor parameter changes
  - Direct contacts to diffusions
- Reliability of through-silicon edits tested
  - Edits robust for design validation

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