A DESIGN EXPERIMENT FOR MEASUREMENT OF THE SPECTRAL CONTENT OF SUBSTRATE NOISE IN MIXED-SIGNAL INTEGRATED CIRCUITS

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ABSTRACT

In mixed-signal ASICs coupling from switching digital nodes and from the digital power supply to analog circuits via the common substrate can degrade the performance of the analog circuits. This paper describes a design experiment to measure the time domain behavior and spectral content of such substrate coupling noise. To measure this noise over a wide frequency range a novel analog substrate noise sensor has been designed. Using this sensor, substrate noise has been measured in the time and frequency domain. Also the influence of supply voltage, switching activity and mounting technique on the substrate noise are experimentally investigated. Simulation results, using a SPICE substrate model, are also included. The presented measurements show that careful investigation of the spectral content of substrate noise is important in the design of mixed-signal ASICs. Differences between the peak noise levels and the noise floor can easily be 40 dB.

I. INTRODUCTION

Substrate coupling in mixed-signal ICs has been identified as a major problem. Accurate simulation of the substrate voltage is necessary to analyze the proper functioning of analog circuits that are integrated on the same substrate as a digital circuit [1]. Nowadays simulation of substrate coupling becomes increasingly important due to the trend to integrate as much circuits as possible on the same die. In recent years a lot of research has been done on modeling the substrate and on substrate coupling reduction techniques. In [2] substrate noise is measured indirectly via the body effect of a single transistor and substrate noise is caused by single inverters with their outputs capacitively coupled to the substrate. Another indirect measurement technique, using voltage comparators, is presented in [3]. Only the noise amplitude and rms value can be measured using that technique. An overview of modeling and simulation techniques can be found in [4] and [5]. Most publications deal with modeling and simulation of substrate noise or with measurements on small test structures, often using an indirect measurement technique. In this paper a versatile substrate coupling experiment, which offers a complete approach to the noise coupling problem, is presented. Using a wideband analog noise sensor, the time domain behavior and spectral content of substrate noise is measured.

First the SPICE substrate model, used for noise simulations, is presented. Then the experiment is described, including the test chip and the analog substrate noise sensor, followed by measurement and simulation results of substrate noise in the time and frequency domain.

II. SUBSTRATE MODELING

The SPICE model used for the substrate depends largely on the type of substrate: low-ohmic or high-ohmic. In case of a low-ohmic substrate the bulk can be considered as one electrical node. For high-ohmic substrates some kind of three dimensional resistor mesh has to be used. For both cases the substrate can be considered purely resistive for frequencies below 10 GHz [6].

The 0.5 μm CMOS twin well technology, in which the experimental chip has been processed, has a low-ohmic substrate with a bulk resistivity of 10-20 $m\Omega cm$. On top of the bulk there is an epi layer of 4 μm thickness with a resistivity of 10-13 Ωcm. The epi layer is modeled by vertical resistors connected to transistor bulk nodes and substrate contacts. The nwell and pwell are about 1 μm thick with a sheet resistance of 1300 Ω. The nwell is modeled by lateral resistors and coupling capacitors to the bulk. The pwell is modeled by lateral resistors. The SPICE substrate model used for the simulations is shown in figure 1, for the example of an inverter. This substrate model is similar to the one presented in [2], except for the extra lateral resistances between bulk nodes and well contacts.

The complete SPICE model of the chip consists of the SPICE description of all analog and digital circuits combined with the substrate model. Inductance of bondwires or flipchip bumps is also taken into account. The SPICE model of the substrate is partly derived by using the layout extraction tool SPACE [7] and partly by manual calculations. For the resistance of a substrate contact or MOSFET

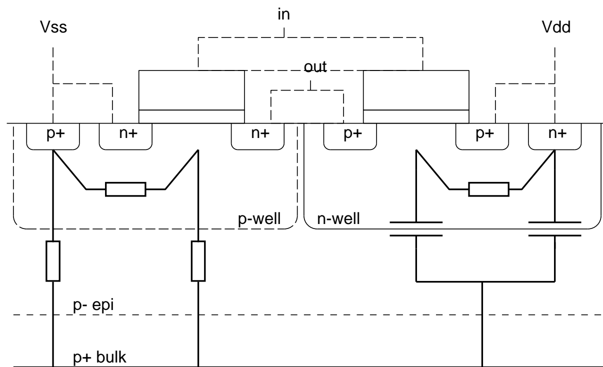

Figure 1: Spice substrate model

bulk connection to the substrate the following expression is used [2]:

$$R_{bulk} \approx R_{area} // R_{perimeter}$$

with

$$R_{area} = \frac{\rho_{epi} T_{epi}}{A} \quad , \quad R_{perimeter} = \frac{\rho_{epi}}{P}$$

A and P are the area and perimeter of a substrate contact or MOSFET gate, T_{epi} is the epi layer thickness and ρ_{epi} is the epi layer resistivity. Lateral substrate resistances can be estimated using the sheet resistance of the particular layer and junction capacitances can be calculated using area and perimeter data of the nwell. For MOSFET modeling the BSIM3v3 model is used, which already includes coupling from the source and drain areas to the bulk connection. In the SPICE circuit description the source and drain geometries extracted from the layout are used.

III. THE DESIGN EXPERIMENT

The mixed-signal test chip is designed in a standard digital CMOS process, with standard digital power rails and IO-pads. The chip contains the following digital circuits: a ring oscillator and clock divider, 3 heavily loaded inverter strings (type 1), 3 less heavily loaded inverter strings (type 2) and 6 pseudo random generators. One heavily loaded inverter strings consists of 7 inverters switched by a latch. Each inverter in the string is loaded by a number of other inverters to increase the coupling to the substrate and to slow down the oscillation of the string. The other string consists of 9 inverters, which are loaded less than in the other string. Each of these 6 strings can be activated individually. One pseudo random generator consists of 9 flipflops and produces a 511 bit pseudo random sequence. Two, four or six pseudo random generators can be activated at the same time.

The analog part consists of two substrate noise sensors: one for calibration purposes and one for the actual measurement of substrate noise. A microphotograph of the core of the mixed-signal chip is visible in figure 2. Surrounding this core are the metal power rails and the

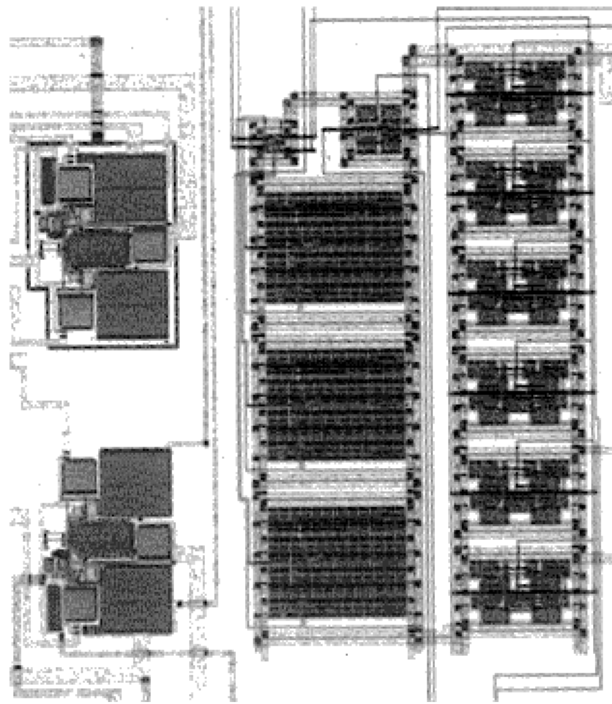

Figure 2: Microphotograph of the core of the test chip

IO-pads. On the left of the photo the two sensors are visible one above the other. The inverter strings are visible in the middle and the pseudo random generators at the right.

The chip has been mounted in two different ways: by wirebond and by flipchip mounting on a Multi Chip Module (MCM) substrate. Digital control signals are connected from a Printed Circuit Board (PCB) to the MCM via wirebonding. Supply voltages, analog outputs and digital clock signals are connected via multi-contact wafer probes to the MCM.

IV. THE SUBSTRATE NOISE SENSOR

The substrate noise sensor is a differential amplifier with one input connected to a quiet ground and the other input connected to the substrate. It has been designed to have a large bandwidth (over 500 MHz) and to deliver a differential output signal in a 50 Ω load. It was not designed to have a large gain because it was expected that the substrate voltage would be large enough to measure without much amplification. The principle schematic of the sensor is shown in figure 3. The coupling capacitors C1 and C2 have been implemented as MOS capacitors, i.e. nMOS transistors with source and drain connected together. For the substrate voltage coupling capacitor, C2, source and drain have been connected to a substrate contact, surrounding the transistor.

The second noise sensor on the test chip has been added

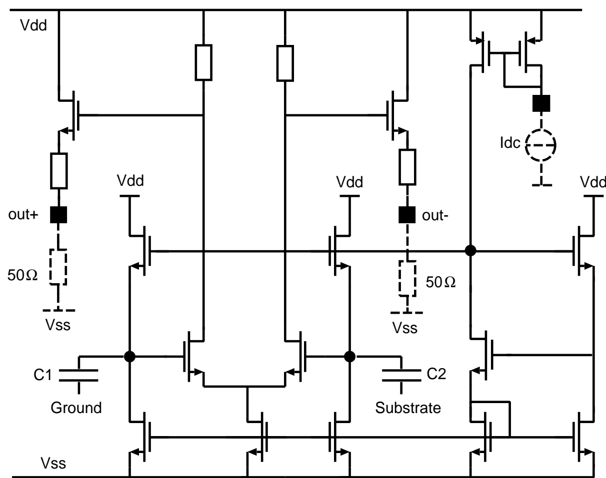

Figure 3: Noise Sensor Schematic

for calibration purposes: this sensor has one input connected to a quiet ground and the other connected to an external voltage source. With this sensor the transfer function can be measured on-chip, using three wafer probes. Figure 4 shows the voltage transfer function. The solid curve shows a number of measurements and the dotted curve represents a SPICE simulation. It can be seen that

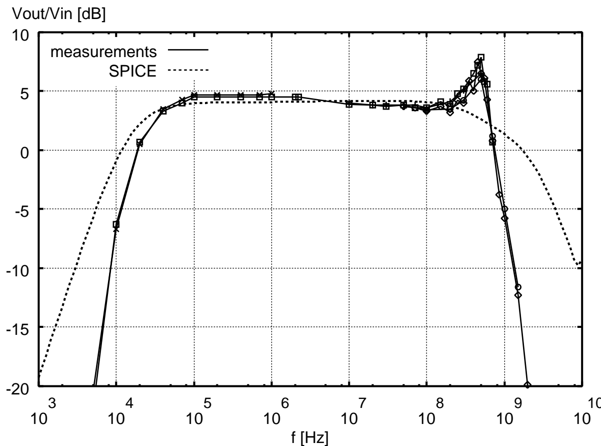

Figure 4: Noise Sensor Transfer Function

the bandwidth of the sensor is 200 kHz to 500 MHz, with an amplification between 3 and 4 dB. Peaking of the amplification around 500 MHz is probably due to the inductance of the probe needles. Differences between the simulation and the measurements at the low and high end of the bandwidth of the sensor are caused by external bias tees in the measurement setup, which have a bandwidth of 100 kHz to 1 GHz.

V. MEASUREMENTS AND SIMULATIONS

In this section the measurement and simulation of the substrate noise is described. First a description of the measurement setup is given followed by time domain and frequency domain substrate voltage measurements and simulations.

A. Setup

The measurement setup is shown in figure 5. The test

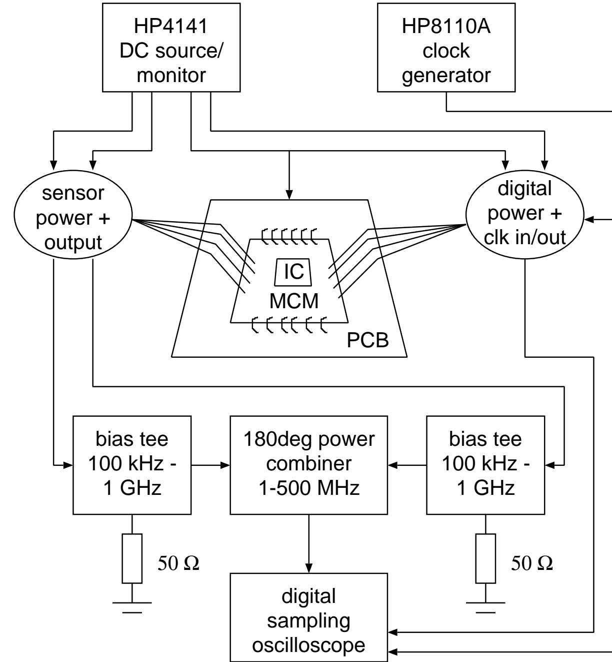

Figure 5: Measurement Setup

chip is mounted on an MCM by means of a wirebond or flipchip technique. The MCM is mounted on a PCB. The digital control signals are wirebonded from the MCM to the PCB. The other connections, power supplies, clock signals and analog outputs, are made via two multi-contact wafer probes.

The differential output of the substrate noise sensor is externally loaded with 50 Ω and AC coupled to a power combiner by means of two bias-tees. The power combiner performs a 180 degrees phase shift for one of its inputs and delivers a single-ended output. This power combiner causes a signal loss of 3 dB, which is approximately compensated by the gain of the noise sensor. In this way the measured output signal corresponds with the substrate voltage. The substrate voltage is measured in the time domain using a digital sampling oscilloscope. Averaging of the substrate voltage over a large number of time domain measurements is performed to decrease measurement noise. This can only be done because the measured substrate voltage is periodical. From this time domain signal the spectrum is calculated by means of a Fast Fourier Transform.

B. Time Domain

First a comparison between the wirebond and flipchip version is made. These results are shown in figure 6. The substrate noise caused by simultaneous switching of 3 heavily loaded inverter strings for a flipchip and wirebond version is shown. Switching of the individual inverters in the string is not visible but instead the measurement shows a sort of integrated switching noise. After the switching of the string has ended ringing occurs. In case of the wirebond version the amplitude of the ringing is larger than in case of the flipchip version. The frequency of this ringing is around 250 MHz. This frequency value can be explained by the combination of the digital circuit capacitance, which is according to SPICE simulations about 75 pF, and the total bondwire inductance, which is typically 4 to 8 nH for two bondwires. Also visible is an oscillation with a much lower frequency, about 6 MHz. This is caused by inductance in the power supply connections in combination with the decoupling capacitor located on the power probe needle.

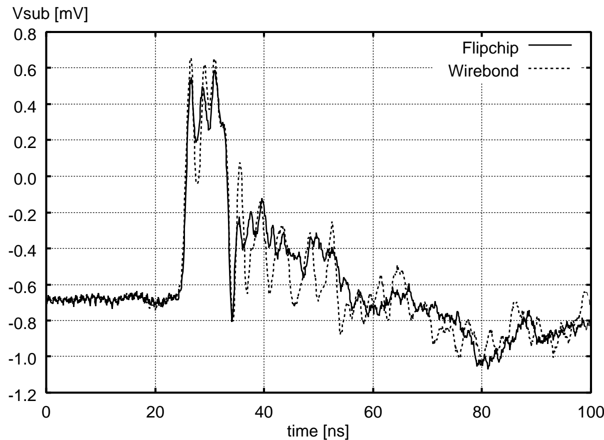

Figure 6: Comparison between the wirebond and flipchip version when switching 3 heavily loaded inverter strings

Next a comparison of a SPICE simulation and measurement of substrate noise for the flipchip version when switching three heavily loaded inverter strings is shown in figure 7. The SPICE simulation has been performed with a power supply inductance of 2 pH and a resistance of 20 $m\Omega$. The simulation result shows the switching of individual inverters, whereas in the measurement a kind of integrated switching activity is visible. This is probably due to the bandwidth of the sensor and the measurement setup. The slow oscillation occuring after the switching activity is also not simulated. This is because not all elements of the measurement setup are included in the SPICE circuit. Therefore simulation of the ringing (at approximately 200 MHz), when including bondwire inductances, results in unrealistic high substrate noise.

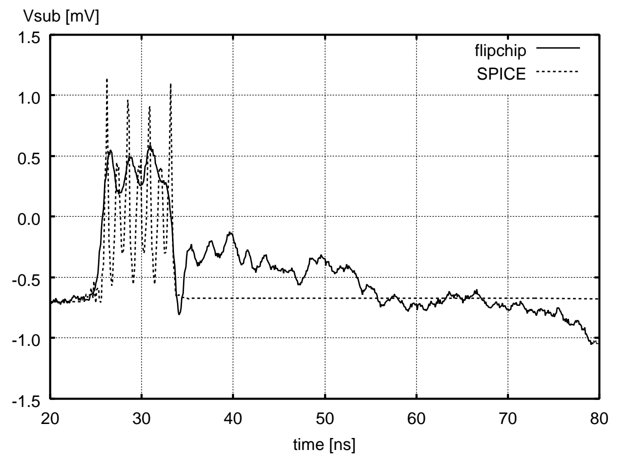

Figure 7: Comparison of measurement and SPICE simulation for the flipchip version when switching 3 heavily loaded inverter strings

The next time domain measurement results are shown in figure 8 and 9. These figures show the peak-to-peak substrate voltage from switching inverter strings for both the wirebond and flipchip version as function of switching activity (number of inverter strings switching simultaneously) and supply voltage respectively. Both figures show that the noise for the wirebond version is always larger than the noise for the flipchip version. Switching noise from inverter string 1 is also larger than noise from string 2. This is because in case of the heavily loaded string more inverters are switched at the same time, which results in a larger coupling to the substrate and a larger power supply current. Those two figures also show that substrate noise, in case of the wirebond version, increases faster with respect to switching activity and supply voltage than in case of the flipchip version. This again illustrates the influence of inductance in the power supply connection on substrate noise.

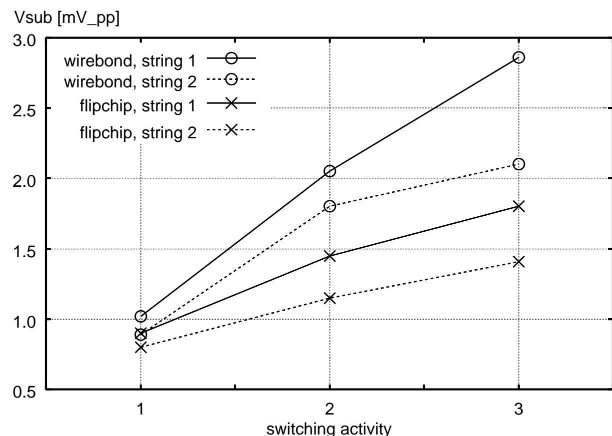

Figure 8: Measured peak to peak substrate voltage as function of digital switching activity for the wirebond and flipchip version

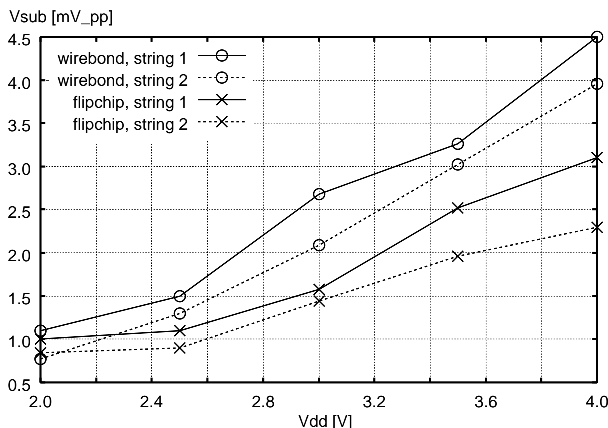

Figure 9: Measured peak to peak substrate voltage as function of digital supply voltage for the wirebond and flipchip version

The last time domain measurement results are shown in figure 10. This figure shows substrate noise caused by switching all six pseudo random generators at 20 MHz. The switching activity is visible over a large period of time so that differences between successive switching instances can been seen. Depending on the number of flipflops that are switching up or down at the same time, the substrate noise is larger or smaller.

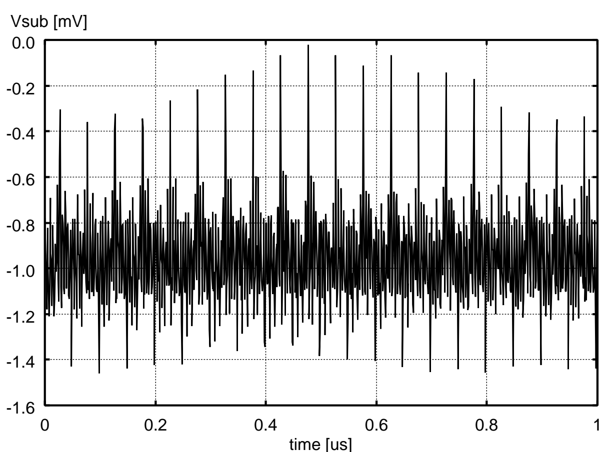

Figure 10: Substrate voltage caused by switching six pseudo random generators for the flipchip version

The behavior of the substrate voltage in the time domain, as shown in the previous plots, can be useful when designing mixed signal ICs. For example, the sampling instance of an analog to digital converter can best be chosen in a “quiet” period, with low substrate noise.

C. Frequency Domain

The first spectral content measurements can be seen in figure 11, showing the frequency spectrum of the substrate noise caused by switching 3 heavily loaded inverter strings at 20 MHz for the wirebond and flipchip version. The vertical scale of this figure indicates the noise voltage amplitude relative to a 1 volt sine wave. Only the part of the spectrum is shown in which ringing is present. In this part of the spectrum differences between the wirebond and flipchip version are clearly visible. Most substrate noise is of course concentrated at the multiples of the clock frequency. But because the inverter string is switched “up” at one edge and switched “down” at the next edge of the 20 MHz clock, this switching activity is repeated at 10 MHz, which is also visible in the measured frequency spectrum.

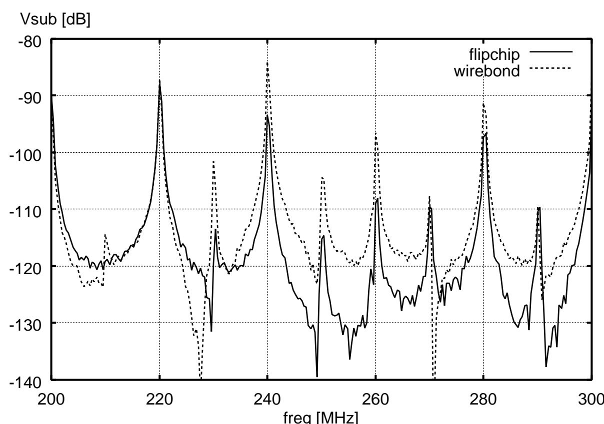

Figure 11: Frequency spectrum of the substrate noise when switching 3 heavily loaded inverter strings for the wirebond and flipchip version

The next measurement results are shown in figure 12. This figure shows the substrate noise frequency spectrum when switching six pseudo random generators at 20 MHz for the wirebond version. Clearly visible is the increase of noise around 200 MHz caused by ringing as mentioned before. Since this switching activity contains no other periodic repetition apart from the 20 MHz clocking (and the

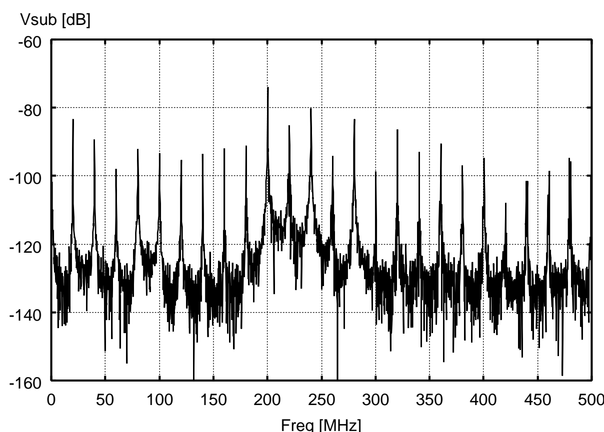

Figure 12: Substrate noise frequency spectrum when switching six pseudo random generators for the wirebond version

low frequency repetition of the pseudo random sequence), all noise peaks are at multiples of the clock frequency.

A detail of the previous spectrum, now also including the flipchip version, is shown in figure 13. The difference

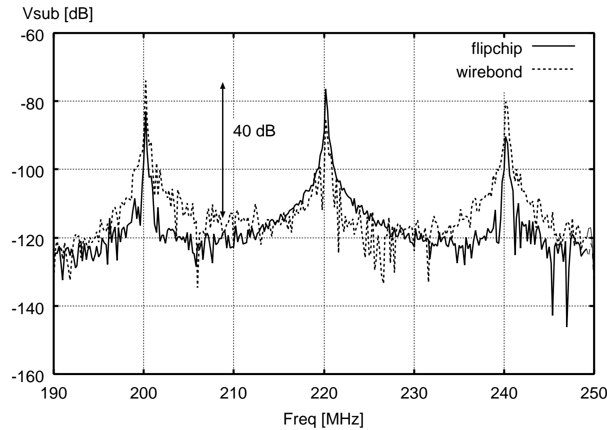

Figure 13: Detail of the frequency spectrum showing substrate noise caused by switching the pseudo random generators for the wirebond and flipchip version

between the wirebond and the flipchip version is much less visible for the switching of the pseudo random generators than for the inverter strings. This is because the ringing is mostly originating from large power supply currents, and in case of the large inverter strings the power supply current is much larger than for the small pseudo random generators.

The previous plots show the importance of investigating the spectral content of substrate noise for designing mixed-signal ICs. Most substrate noise is concentrated at multiples of the clock frequency and the difference between the peak noise levels and the noise floor can be easily 40 dB. Analog channels, for example for intermediate frequencies of RF transceivers, can best be located between the noise peaks.

More measurements on the test chip are still in progress. Measurement of power supply noise and the study of several power supply decoupling techniques have still to be performed. The presented noise sensor will also be included on some future digital designs, to measure the spectral content of the substrate noise of larger digital circuits.

VI. CONCLUSIONS

In this paper a novel method of measuring substrate noise has been presented. A differential amplifier with a large bandwidth has been used to allow measurements of substrate noise in the time and frequency domain. Time and frequency domain measurements, using this substrate noise sensor, have been performed on inverter strings and pseudo random generators. Also the influence of switching activity, power supply voltage and mounting technique on the substrate noise has been shown. A SPICE substrate model has been presented that is used for substrate noise simulations. The importance of investigating the time domain behavior and the spectral content of substrate noise when designing mixed-signal ICs has been shown. For our digital circuit a difference between peak noise levels and noise floor of 40 dB has been observed.

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