

# Analysis and Experimental Verification of Digital Substrate Noise Generation for Epi-Type Substrates

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**Abstract**—Substrate coupling in mixed-signal IC's can cause important performance degradation of the analog circuits. Accurate simulation is therefore needed to investigate the generation, propagation, and impact of substrate noise. Recent studies were limited to the time-domain behavior of generated substrate noise and to noise injection from a single noise source. This paper focuses on substrate noise generation by digital circuits and on the spectral content of this noise. To simulate the noise generation, a SPICE substrate model for heavily doped epi-type substrates has been used. The accuracy of this model has been verified with measurements of substrate noise, using a wide-band, continuous-time substrate noise sensor, which allows accurate measurement of the spectral content of substrate noise. The substrate noise generation of digital circuits is analyzed, both in the time and frequency domain, and the influence of the different substrate noise coupling mechanisms is demonstrated. It is shown that substrate noise voltages up to 20 mV are generated and that, in the frequency band up to 1 GHz, noise peaks are generated at multiples of the clock and repetition frequency. These noise signals will strongly deteriorate the behavior of small signal analog amplifiers, as used in integrated front-ends.

**Index Terms**—Amplifiers, CMOS integrated circuits, crosstalk, integrated circuit modeling, interference, mixed analog–digital integrated circuits, substrate noise.

## I. INTRODUCTION

SUBSTRATE coupling in mixed-signal IC's has been identified as a major problem due to the trend to integrate as many circuits as possible on the same die. Accurate simulation of the substrate voltage is necessary to analyze the proper functioning of analog circuits that are integrated on the same substrate as a digital circuit [1]. These simulations give insight in the time and frequency domain behavior of substrate noise. This information is very useful when designing mixed-signal ASIC's: low substrate noise time periods and frequency bands can be identified and used for sensitive analog signal operations.

In recent years a lot of research has been done on modeling the substrate and on substrate coupling reduction techniques [2]–[4]. Most publications deal with modeling and simulation of substrate noise propagation in the time domain or with measurements on small test structures, often using indirect measurement techniques.

In this paper a substrate modeling strategy is presented which allows accurate simulation of the time and frequency domain be-

havior of substrate noise generated by digital circuits. To verify these simulations, a test chip has been designed, containing a substrate noise sensor, which allows continuous-time wide-band measurement of substrate noise.

First the different sources of substrate noise are discussed. Next the substrate model is described that is used in the SPICE simulations, followed by a description of different substrate noise measurement techniques. Finally, measurements and simulations in the time and frequency domain are presented, together with an analysis of the dominant sources of substrate noise.

## II. SOURCES OF SUBSTRATE NOISE

All current injected into the substrate will cause fluctuations of the substrate voltage. This is called substrate noise and is caused by coupling of switching or noisy signals to the substrate. In digital CMOS circuits this noise is caused by three mechanisms: coupling from the digital power supply, coupling from switching source–drain nodes and impact ionization in the MOSFET channel. Noise on the digital power supply is caused by  $di/dt$  noise and resistive voltage drops due to the inductance and resistance in the power-supply connections to the chip. The combination of the inductance in the power-supply connection and the on-chip capacitance between power and ground will also cause ringing of the power-supply voltage. These effects are also called ground bounce or simultaneous switching noise [5]–[7]. Typically, the digital ground is connected to the substrate in every CMOS gate, which results in a very low resistance between digital ground and substrate, and all digital ground noise and ringing will also be present on the substrate. Therefore, this noise coupling mechanism is often the dominant cause of substrate noise.

The second origin of substrate noise is capacitive coupling from switching source and drain nodes of the MOSFET's. The resulting substrate voltage waveform will show the same characteristics as the switching signals on the source–drain nodes. For noise coupling from the power supply this is not the case: a switching gate will cause an increase of the ground voltage, which causes a positive noise peak on the substrate.

The third source of substrate noise is impact ionization [8]. Whether or not impact ionization is an important source of substrate noise depends on the technology, especially on the combination of the supply voltage and channel length. According to the transistor models provided by the foundry, the substrate current caused by impact ionization was negligible for the 0.5- $\mu\text{m}$  3.3-V CMOS technology used in our experiments.

Manuscript received December 9, 1999; revised January 26, 2000. This work was supported in part by the Flemish IWT project FRONTENDS and the ESPRIT project BANDIT.

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Publisher Item Identifier S 0018-9200(00)03868-3.

The influence of the different noise sources and the relation with the power-supply connection inductance will be shown later, when discussing the experimental results, in more detail.

### III. SUBSTRATE MODELING

To simulate substrate noise, a model of the substrate is necessary. These models vary from complicated electromagnetic models to simple lumped-element models. For epi-type substrates the heavily doped bulk can be considered as one electrical node and only the resistance of the epi layer has to be taken into account [2]. This results in a simple lumped-element model. Our test chips have been processed in a 0.5- $\mu\text{m}$  CMOS twin-well technology with a low-ohmic (10 m $\Omega\cdot\text{cm}$ ), epi-type substrate, and a single node substrate model will be used for the simulations.

To accurately simulate substrate noise generation, the three different sources of substrate noise must be included in the model. The coupling from the power supply has to be included in the substrate model by adding resistors from the substrate contacts connected to the digital ground to the substrate bulk node. Also the capacitive coupling via the n-well junction capacitance from the positive power supply to the substrate must be included. The coupling from switching source–drain nodes and impact ionization is handled by the MOSFET model (the BSIM3v3 model). For the SPICE description of the digital circuit a layout parasitics extraction (LPE) file has been used that includes parasitics of the interconnect. Also the external parasitics in the power-supply connection, such as bondwire inductances (e.g., using the 1 nH/mm rule) and external decoupling capacitors are taken into account.

Our substrate model is based on the model presented in [2], but lateral resistances between MOSFET bulk nodes and nearby well contacts have been added. These lateral resistances are important, because they will reduce coupling from source–drain nodes and at the same time increase coupling from the power supply to the substrate. This is especially the case in twin-well technologies, which have an n-well and p-well that are more heavily doped than the epi layer. The SPICE substrate model used for the simulations is shown in Fig. 1, for the example of a CMOS inverter. The vertical resistances in the SPICE substrate model are calculated using an approximate expression that states that the total resistance of a substrate contact consists of the parallel combination of the resistance of a rectangular block and hemisphere [2]

$$R_{\text{epi}} \approx \frac{\rho_{\text{epi}} t_{\text{epi}}}{A} \parallel \frac{\rho_{\text{epi}}}{P} \quad (1)$$

with  $\rho_{\text{epi}}$  and  $t_{\text{epi}}$  the resistivity and thickness of the epi layer and  $A$  and  $P$  the area and perimeter of the substrate contact or MOSFET gate. The resistance values obtained with this equation match well with extracted substrate resistances, using the tools SPACE [9] and LAYIN [10]. The lateral resistances between well contacts and MOSFET bulk nodes are estimated using the well sheet resistance. N-well junction capacitances are calculated using the technology data and well geometry. Noise coupling from other structures, like bondpads, can be easily added to this model by including a capacitor (for the field oxide)

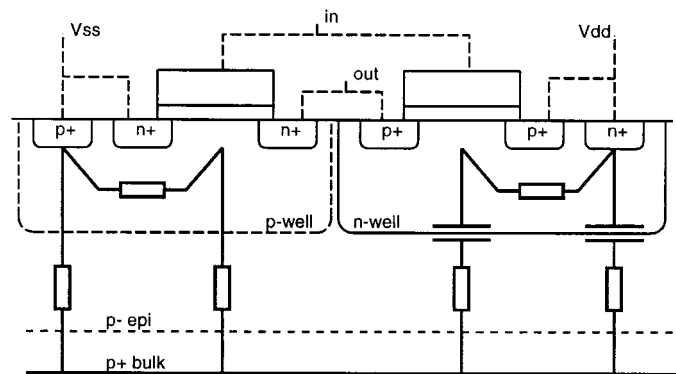


Fig. 1. Substrate resistors and well capacitors that form the SPICE substrate model.

with series resistance (for the epi layer) connected to the substrate node.

### IV. SUBSTRATE NOISE MEASUREMENT TECHNIQUES

The method of generation and measurement of substrate noise is important to verify the accuracy of the substrate models and noise simulations. This section will describe some existing measurement techniques, followed by the description of our analog substrate noise amplifier. Also the details of the digital substrate noise generation circuit will be presented.

#### A. Measurement Techniques

A simple measurement technique, used in a number of publications, involves the use of the threshold voltage modulation of a single MOSFET [2], [11]. Also voltage comparators can be used as noise sensors [12], [13]. Both are indirect measurement techniques: not the substrate voltage is measured but the influence of the substrate voltage on the MOSFET current or comparator state.

A continuous-time direct measurement technique is the use of an analog differential amplifier, with one input connected to the substrate and the other to a quiet reference signal [14], [15]. The sensor presented in [14], however, has only a limited bandwidth, and measurement of actual coupling from switching digital nodes is not possible due to this bandwidth limitation. A method for accurate measurement of substrate noise up to 1 GHz, as presented in [15], is analyzed in more detail below.

#### B. Differential Substrate Noise Amplifier

The substrate noise sensor used in our experiments is a differential amplifier with one input connected to a quiet ground and the other input connected to the substrate. Main objectives during the design have been a large bandwidth (over 500 MHz) and the ability to deliver a differential output signal in a 50- $\Omega$  external load. The schematic of the sensor is shown in Fig. 2. The coupling capacitors C1 and C2 have been implemented as large finger-structured MOS capacitors (W/L = 2000/1). For the substrate voltage coupling capacitor C2, source and drain have been connected to a substrate contact, surrounding the transistor. The source and drain nodes of capacitor C1 have been connected via a dedicated connection, off-chip to the analog ground. Like the circuit, the layout has been made as symmetrical as possible.



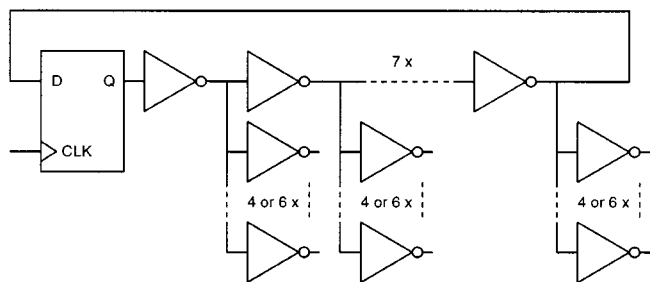


Fig. 5. Inverter chain noise generation circuit.

a less heavily loaded and a more heavily loaded version. The SPICE description of this circuit consists of the digital gates, the extracted interconnect parasitics, and the substrate resistors and well junction capacitors, added according to the model presented in Section III.

## V. EXPERIMENTAL RESULTS

The measurements have been performed on a mixed-signal test chip, which contains several digital circuits for the noise generation and substrate noise sensors for the noise measurements. Both the digital and analog signals and power supplies are directly connected to the chip, using multicontact wafer probes [16]. The probe needles for supplying the power to the chip contain a 22-nF decoupling capacitor, located near the point of the needles. This measurement setup makes it possible to measure the generated substrate noise of the digital circuits, without the influence of bondwires or other package parasitics. In all experiments the differential output signal of the sensor is being measured and corrected for the 3-dB amplification of the sensor to derive the actual substrate voltage.

### A. Time-Domain Substrate Noise

Measurements have been performed in the time domain to study the amplitude and duration of the substrate noise signal generated by the inverter chain. SPICE simulations have been performed to study the validity of the substrate model. For accurate noise simulations, the wafer probe elements have to be added to the SPICE description of the IC. These are shown in Fig. 6. The wafer probe elements are a decoupling capacitor of 22 nF with a small parasitic series resistance and some small parasitic inductances. The probe-to-supply connection is considered as a very low impedance circuit due to further decoupling. The parasitic component values are determined by fitting simulation and measurement results, but agree reasonably well with the expected parasitics of the wafer probe.

Fig. 7 shows the measurement and the corresponding SPICE simulation. From 8-ns to 16-ns substrate noise is generated by the switching inverters. Visible are the seven noise peaks corresponding to the switching of the seven stages in this inverter chain. The supply current for this switching activity is mainly delivered by the 22-nF decoupling capacitor. The dc-offset in the substrate noise signal is caused by the series resistance of this capacitor. Due to this resistor, power-supply noise coupling is dominant, as indicated by the seven noise peaks (instead of seven edges). The relation between the substrate noise waveform and the dominant coupling mechanisms is explained next.

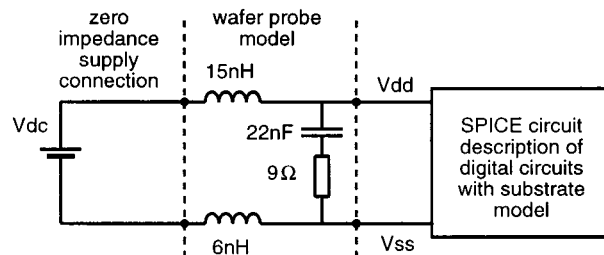


Fig. 6. Parasitics of the measurement setup that have been added to the SPICE simulation model.

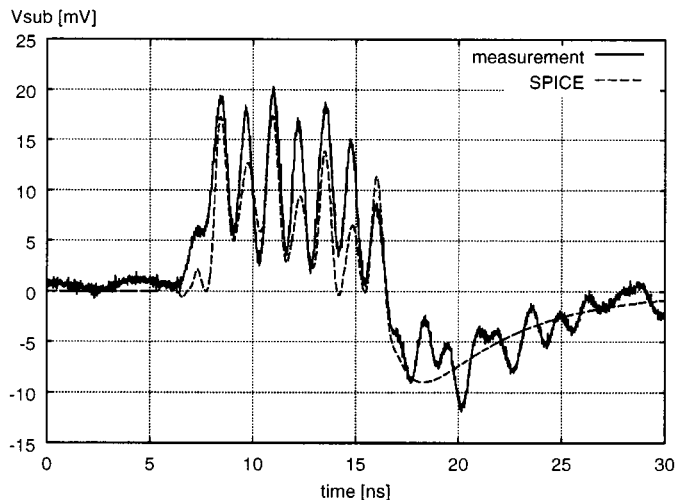


Fig. 7. On-chip measurement and simulation of substrate noise caused by switching the 7-stage inverter chain.

The agreement between measurements and simulations is very good. Therefore further simulations can be done with reliable results.

### B. Dominant Noise Coupling Source Analysis

To show the effect of only an external parasitic inductor (e.g., from a wirebond connection) on the shape and amplitude of the generated substrate noise signal, a SPICE simulation has been performed with a 0 nH, 1 nH, and 10 nH external inductor in the power-supply connection. The SPICE simulation model of Fig. 6 has been used, without the wafer probe model but with an equal inductance (of 0, 1, or 10 nH) in the power and ground lines. These simulations are shown in Fig. 8. The 0-nH simulation shows the minimum amount of substrate noise that will be generated by capacitive coupling from the source and drain nodes. This substrate noise level can only be reduced by increasing the number of substrate contacts to the quiet digital ground. The simulation with the 1-nH inductor shows a much larger substrate noise signal, now dominated by noise coupling from the power supply. For even larger inductance values (10 nH), the maximum substrate noise will be caused by ringing of the damped LC tank, formed by the inductance and the on-chip capacitance with series resistance over the power supply.

To provide more insight in the dominant source of substrate noise, the peak-to-peak substrate voltage, generated by the inverter chain, has been analyzed as function of the inductance, for a substrate model that only includes coupling

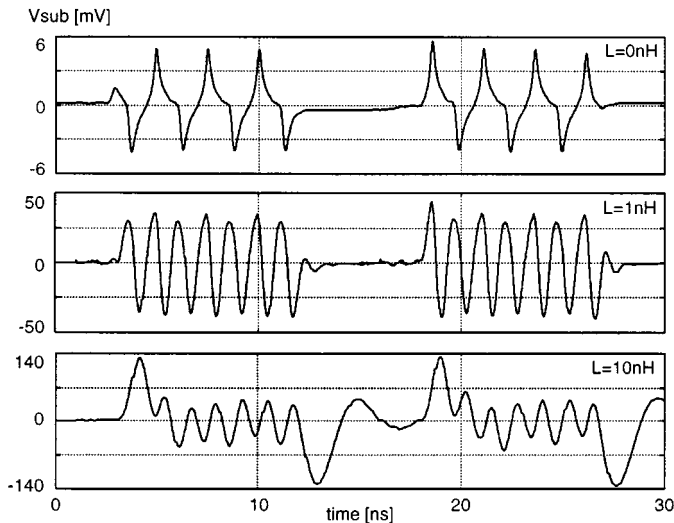


Fig. 8. Simulated substrate noise for 0 nH, 1 nH, and 10 nH, showing the different sources of substrate noise.

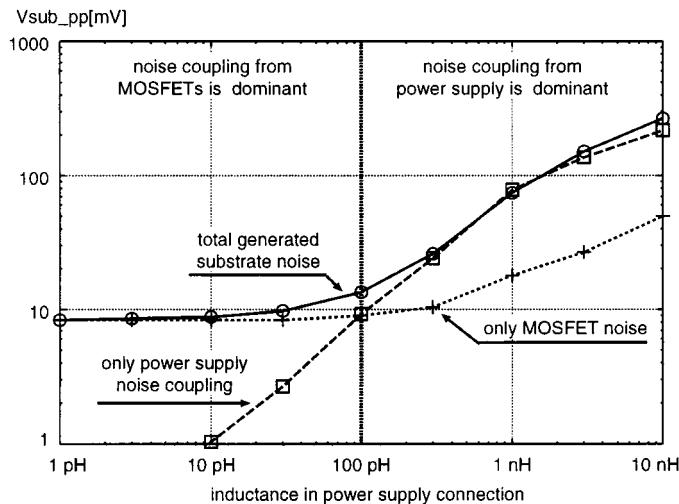


Fig. 9. Simulated peak-to-peak substrate voltage versus the inductance of the power-supply connection to the chip.

from the MOSFET source and drain nodes, for a model that only includes coupling from the power supply, and for the total substrate model. The results are shown in Fig. 9. For the simulations with only noise coupling from the MOSFET's, the substrate and wells have been connected to a quiet (dedicated) power supply. This situation can also be realized in reality and, as will be shown, is a useful way to reduce the substrate noise. For low inductances the generated noise is almost constant. When the noise on the power supply increases with increasing inductance, the substrate noise also increases due to capacitive noise coupling from source and drain nodes that are directly connected to the noisy  $V_{dd}$  or  $V_{ss}$ . For the simulations with only power-supply noise coupling, the bulk nodes of the MOSFET's have been directly connected to a quiet power supply. For low inductances the substrate noise increases linearly with the inductance. At higher inductance values the maximum substrate noise is dominated by ringing of the power supply that couples to the substrate. The simulation with the complete substrate

model clearly shows that for this circuit noise coupling from the MOSFET's is dominant up to 100-pH inductance and that the power-supply noise coupling is dominant for higher inductance values. This is important information when choosing between flip-chip connections, with a typical inductance around 30 pH, and wirebond connection, with an inductance between 2 nH and 10 nH.

From this analysis it can be concluded that the substrate noise generation of a digital circuit can be reduced by reducing the value of the power-supply connection inductance. Only when the power-supply noise is not dominant anymore, the substrate noise can be further reduced by increasing the number of substrate contacts (i.e., reducing the resistance between the substrate and the digital ground). Increasing the number of substrate contacts, when power-supply noise coupling is dominant, will only increase the noise coupling from the noisy power supply to the substrate. Using a dedicated substrate and well bias, with low connection impedance, is also an effective way to reduce the noise generation.

### C. Frequency Domain Substrate Noise

Studying substrate noise in the frequency domain can also reveal important information about the sources of the noise and can give useful information when designing mixed-signal circuits (e.g., during frequency planning for a receiver front-end).

The spectral content measurements have been performed using the two versions of the inverter chain. By comparing the measurements of the slow (heavily loaded) and faster (less loaded) switching inverter chain, the influence of the switching frequency on the substrate noise generation in the frequency domain can be shown.

The two measured spectra are shown in Fig. 10, with the heavily loaded version at the top and the less loaded at the bottom of the figure. In both cases the circuits are clocked at 20 MHz. At low frequencies, up to a few hundred MHz, the substrate noise is concentrated at multiples of the 20-MHz clock signal. Parasitic effects such as ringing of the power supply will cause an extra increase of substrate noise in this frequency range. Noise coupling from the inverter chains causes noise peaks at multiples of half the clock frequency, due to the divide-by-2 behavior of the circuit. SPICE simulations of the switching inverter chain show that, for the heavily loaded version, the noise coupling from the switching source-drain nodes is most dominant around 360 MHz, which corresponds to the switching frequency of the ring oscillator. The noise coupling from the power supply is most dominant at twice this frequency, 720 MHz. At both these regions a strong increase in substrate noise amplitude can be seen, but the largest contribution is from the power-supply coupling around 720 MHz.

Also for the less loaded inverter chain the dominant source of substrate noise from the switching inverters comes from power-supply noise coupling, which occurs around 1080 MHz. A minor contribution from the switching source-drain nodes is visible at 540 MHz. Again, both switching frequencies are extracted from SPICE simulations.

From these measurements it can be concluded that substrate noise is concentrated at multiples of the digital clock frequency

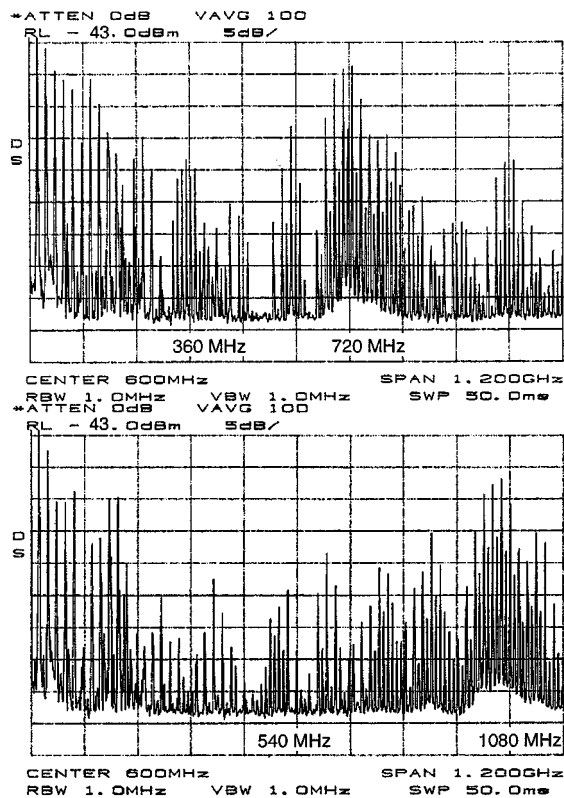


Fig. 10. Measured spectral content of substrate noise from 0 to 1.2 GHz, generated by the heavily loaded (top) and less loaded (bottom) inverter chain clocked at 20 MHz (reference level  $-43$  dBm or 1.58 mV).

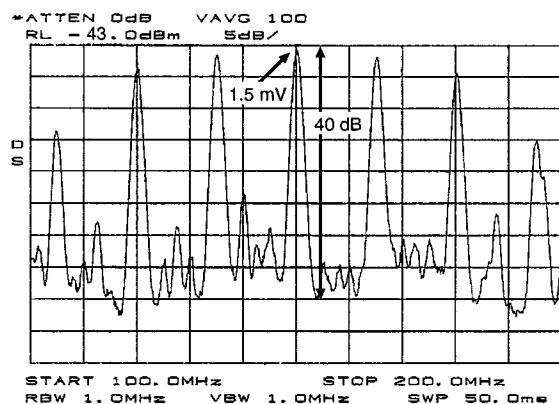


Fig. 11. Measured substrate noise from 100 MHz to 200 MHz caused by the heavily loaded 7-stage inverter chain clocked at 15 MHz (reference level  $-43$  dBm or 1.58 mV).

and multiples of the repetition frequency of the circuit (in our case half the clock frequency). These noise peaks occupy the entire spectrum, but the amplitude is influenced by the noise coupling mechanisms. These results show that, when power-supply noise coupling is dominant, the clock-related substrate noise is much more relevant than gate-delay related noise, as described in [17], where power-supply noise coupling was not taken into account.

When designing mixed-signal integrated circuits, such as an integrated analog IF or RF front-end stage together with a base-band digital modem, it is important to take the frequency and amplitude of the major substrate noise spectral components into

account. This is illustrated in Fig. 11. This figure shows the measured spectrum of substrate noise from the heavily loaded inverter chain clocked at 15 MHz, in the frequency range from 100 MHz to 200 MHz. It can be seen that substrate noise signals as high as 1.5 mV are generated at multiples of the clock frequency and that the substrate noise peaks are 40 dB above the measurement noise floor, which can seriously degrade analog amplifier behavior.

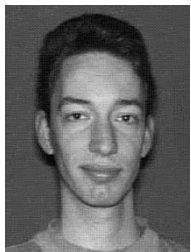
## VI. CONCLUSIONS

The presented substrate noise sensor has proven to be a valuable tool in the investigation of substrate noise. It allows continuous-time wide-band measurements of substrate noise up to 1 GHz, which is necessary for determining the spectral content of substrate noise and checking the validity of the substrate model. The simulated substrate noise waveforms have shown good correspondence with the measurements, although the results are still dominated by external parasitics. It has been shown that, for small power-supply connection inductances, the substrate noise has a certain minimum value, and that for larger inductance values, power-supply noise will be the dominant source of substrate noise. The measured spectra of the substrate noise have shown that most substrate noise is concentrated at multiples of the digital clock frequency and repetition frequencies of the circuit. At these frequencies substrate noise signals are generated as high as 1.5 mV, and the substrate noise peaks are 40 dB above the measurement noise floor. This indicates the importance of a good selection of digital clock frequency and analog IF frequencies (frequency planning) in integrated transceiver front-ends.

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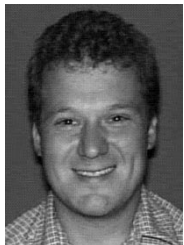
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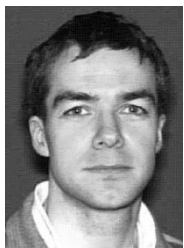
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Dr. Bolsens was the recipient in 1986 of the Darlington Award of the IEEE Circuits and Systems Society with the citation "Best paper published by the IEEE CAS Society that bridges the gap between theory and practice." He received a distinguished paper citation at the 1991 International Conference on CAD. In 1993 he received a best circuit award from the EUROASIC-EDAC conference.