

22.1 Substrate Noise Generation in Complex Digital Systems: Efficient Modeling and Simulation Methodology and Experimental Verification

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More and more system-on-chip designs require the integration of analog circuits on large digital chips and therefore suffer from substrate noise coupling. To investigate the impact of substrate noise on the analog circuits, information is needed about digital substrate noise generation. A methodology for modelling and simulating the time-domain waveform of the generated substrate noise of large digital circuits is verified with measurements on an 86kgate CMOS ASIC. The difference between simulated and measured substrate noise RMS voltage is <10% and simulation time is of the same order of magnitude as a gate-level VHDL simulation. For smaller circuits, e.g., a 1kgate multiplier, a speedup in simulation time of 3 orders of magnitude is obtained with respect to a full SPICE simulation.

Whereas most publications deal with substrate noise generation of relatively small digital circuits, e.g., full adders [1], this test chip consists of an 86kgate digital circuit and analog substrate noise sensors to measure the substrate noise voltage [2]. The digital circuit is a multi-rate up/down converter and channel select filter for cable modem applications [3]. This chip can up-convert or down-convert 12b I/Q data by a factor of 16 and perform channel selection. Figure 22.1.1 shows the micrograph and specifications of this chip and also the location of the analog substrate noise sensors. The schematic and measured and simulated transfer functions of these sensors are shown in Figure 22.1.2. The sensors amplify the substrate voltage by 3dB in the frequency band from 20kHz to 1GHz [2].

The model used for the substrate noise simulations is shown in Figure 22.1.3. It includes noise generation from core cells, IO cells, power supply pads and package parasitics. Macro models of the core cells, IO cells and supply pads take into account the impedance between the power supply and substrate nodes. The low-ohmic substrate is modeled as a single node and all core and IO cell models are placed in parallel [4]. Figure 22.1.3 shows the element values for the parallel combination of all core and IO cell models. Macro models are extracted once for an entire standard-cell library with SPICE simulations that include a detailed substrate model obtained with SubstrateStorm [5]. Substrate noise generation is modeled by current sources that represent noise injection by switching gates ($I_{sub,core}$ and $I_{sub,IO}$) and power supply current consumption (I_{vdd} , I_{vss} , I_{vddc} and I_{vssc}), calculated from switching events that are extracted from a VHDL gate-level simulation.

Since the package parasitics, such as bondwire, trace, and pin inductance and resistance, determine a large part of the substrate noise generation, it is important to determine accurate values for these parasitics. For this 120-pin ceramic pin grid array package, an average value of 12nH in series with 1.5Ω is measured for one connection. The parasitic inductance in the power supply, which consists of 8 parallel connections, in combination with the total on-chip capacitance between power and ground (around 3.5nF), causes ringing at a frequency of ~40MHz. This ringing also couples to the substrate and causes a 20dB increase of substrate noise around that frequency.

Measurement of the RMS substrate noise voltage versus clock frequency and supply voltage, in Figure 22.1.4, shows that it scales with the square root of the clock frequency and linearly with the supply voltage. This means that substrate noise power scales in the same way, and is closely related to, dynamic power consumption. The measured time waveform of the substrate noise voltage and the frequency spectrum of this signal are shown in Figure 22.1.5 and 22.1.6. For this specific circuit operation, the RMS substrate noise voltage is 13.3mV. The largest substrate noise peak in the frequency spectrum is -46dBV (5.0mV) and is generated at the master clock frequency (50MHz). 62% of the total substrate noise power is generated at multiples of the lowest clock frequency (3.125MHz).

Simulation results of the substrate noise generation are shown in Figure 22.1.5 and 22.1.6 and compared with the measurements. The difference between measured and simulated RMS substrate voltage is <10%. From the simulations it can be determined that, for this circuit operation with data output at 50MHz, only 18% of the total noise power is generated by the switching IO buffers. For down-conversion, with data output at 1.56MHz, this is only 7%. This means that most substrate noise is generated by simultaneous switching activity of core cells (mainly flip-flops), which therefore needs to be carefully modeled. Table 22.1.1 gives an overview of the simulation times for this circuit and for a smaller example. The substrate noise simulation time for this circuit is about the same as the VHDL gate-level simulation time. Comparison with a full SPICE simulation of the digital circuit with its substrate model is not feasible due to the circuit size. For a 1kgate circuit, the speedup with respect to a full SPICE simulation is >1500 times.

An efficient simulation methodology for substrate noise generation of large digital circuits shows simulated RMS substrate noise voltage that differs <10% from measurements on an 86kgate CMOS ASIC. Simulation time is about the same as the VHDL gate-level simulation time.

References:

- [1] Nagata, M., et al., "Reduced Substrate Noise Digital Design for Improving Embedded Analog Performance," ISSCC Digest of Technical Papers., pp. 224-225, Feb. 2000.
- [2] van Heijningen, M., et al., "Analysis and Experimental Verification of Digital Substrate Noise Generation for Epi-Type Substrates," IEEE J. Solid-State Circuits, vol. 35, no. 7, pp.1002-1008, July, 2000.
- [3] Pasko, R., et al., "High-Performance Flexible All-Digital Quadrature Up and Down Converter Chip," IEEE Custom IC Conf., pp.43-46, 2000.
- [4] van Heijningen, M., et al., "High-Level Simulation of Substrate Noise Generation Including Power Supply Noise Coupling," Proc. 37nd Design Automation Conference, pp.446-451, 2000.
- [5] SubstrateStorm, <http://www.simplex.com/solutions/products/substratestorm.html>

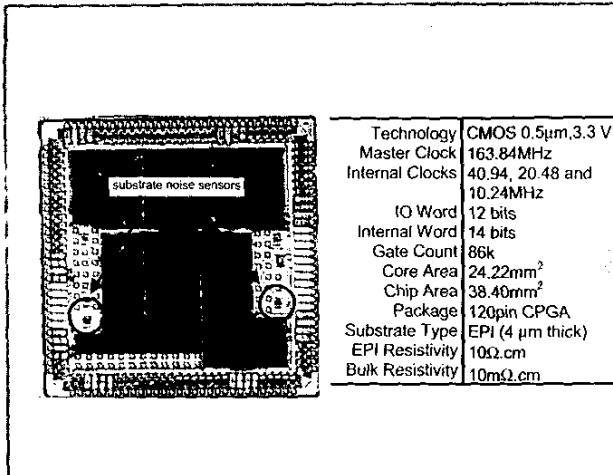


Figure 22.1.1: Micrograph of the Robo4 chip and specifications.

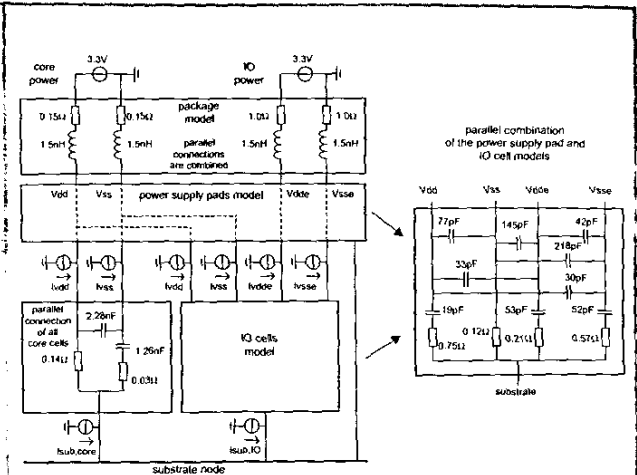


Figure 22.1.3: Simulation model for substrate noise calculations.

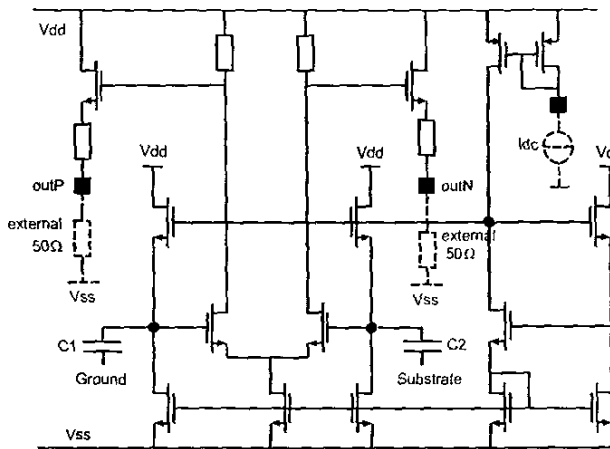


Figure 22.1.2: Schematic and transfer function of the substrate noise sensor.

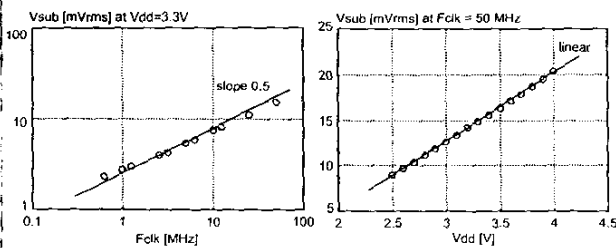
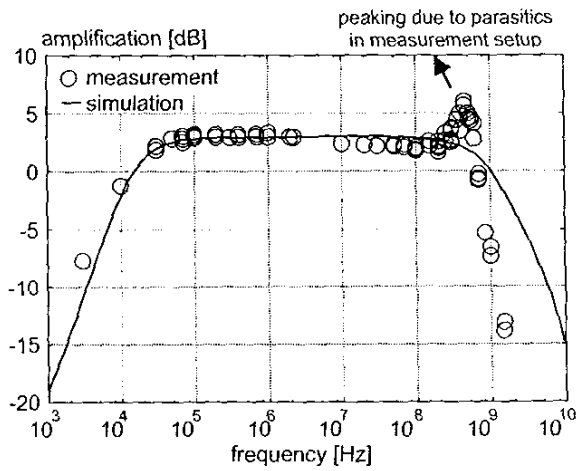


Figure 22.1.4: Measured substrate noise versus clock frequency and supply voltage.

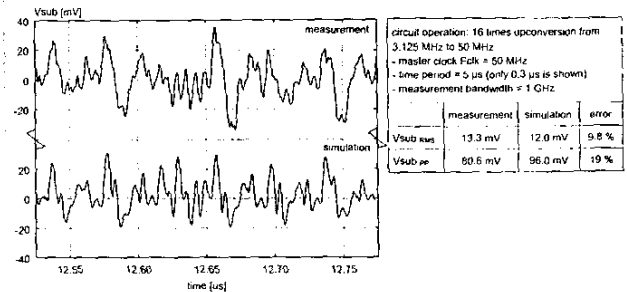


Figure 22.1.5: Comparison of measured and simulated substrate noise waveforms.

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Comparison for the same protocol/burst overhead and an uncoded data rate of 76 Mb/s	Festival [3] QPSK ASIC	Carnival 64-QAM ASIC	Advantage for Carnival if > 1
Efficiency	1.5b/s/Hz	3.8b/s/Hz	2.5
Energy per transmitted bit	8.8nJ/b	2.6nJ/b	3.4
Energy per received bit	7.5nJ/b	2.8nJ/b	2.7
Transmit power	670mW	199mW	3.4
Receive power	570mW	212mW	2.7
Max. clock frequency	50MHz	20MHz	2.5
Technology	0.35µm CMOS	0.18µm CMOS	-
Voltage	3.3V	1.8V/3.3V	-
Die size	16.4mm ²	20.8mm ²	0.7

Figure 21.5.6: The 64-QAM carnival ASIC shows performance gains over the previous QPSK ASIC in all categories except for a moderate die size increase.

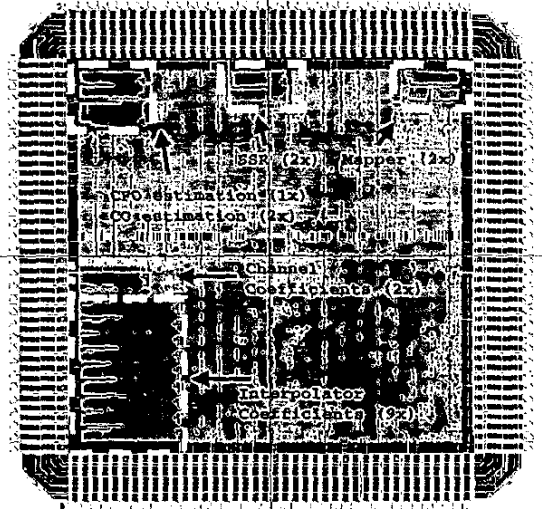


Figure 21.5.7: Chip layout view with RAMs highlighted.

Module	Power Budget
Tx chain	290mW
Rx chain	540mW
ADC	2 x 155mW
DAC	2 x 58mW
Reference Generator	145mW

Table 21.6.1: Power budget.

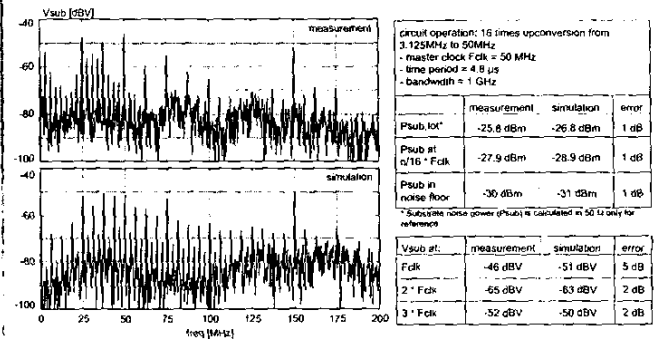


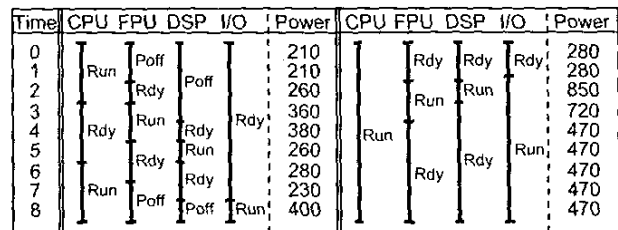
Figure 22.1.6: Frequency spectrum of measured and simulated substrate noise voltage.

	Robo4	multiplier
	86 K gates	994 gates
Simulated time	1µs	5µs
No. switching events	150k	63.5k
Clock frequency	50MHz	42MHz
Full SPICE-level simulation	---	37 hours
VHDL gate-level simulation	11:27 min	29s
Substrate noise simulation	12:30 min	55s
Speedup	---	1586x

Table 22.1.1: Overview of simulation times.

	Running (Run)	Ready (Rdy)	Power off (Poff)
Block A (CPU)	200mW	50mW	0mW
Block B (FPU)	300mW	50mW	0mW
Block C (DSP)	150mW	20mW	0mW
Block D (I/O)	200mW	10mW	0mW

(a) PTAB, assuming chip consists of four blocks.



(b) ChipOS (Pmax = 400 mW)

(c) Conventional

Figure 22.2.7: Example of power scheduling.