

BANDIT: EMBEDDING ANALOG-TO-DIGITAL CONVERTERS ON DIGITAL TELECOM ASICS

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ABSTRACT

This paper summarizes the objectives and some early results of the ESPRIT project 29260 BANDIT. It is a 3 year project that started in September 1998. Coordinating partner is IMEC and the other partners are K.U.Leuven and Ericsson Radio Systems (ERA). The goal of BANDIT is to develop a general design and test methodology for embedding high-speed analog/digital converters (ADCs) on large digital telecom ASICs, with special attention to the problems caused by mixed-signal integration, such as substrate noise coupling. After an overview of the project objectives the first results in the field of substrate noise coupling analysis are presented.

1. INTRODUCTION: PROJECT OBJECTIVES

The goal of BANDIT is to develop a general design and test methodology for embedding high-speed analog/digital converters on large digital telecom ASICs, with special attention to the problems caused by mixed-signal integration. Techniques will be investigated to analyze and model digital noise generation and its impact on ADC performance. Design techniques will be developed to reduce the noise generation as well as the impact of digital noise on the performance of the ADC. A general design for test methodology will be developed for high-speed mixed-signal ASICs consisting of a high-speed ADC and a fast, multirate digital signal processing (DSP) block. The developed methodologies will be demonstrated and evaluated by means of an integrated circuit design for a wireless local area network (WLAN) modem.

Another objective is to investigate the limits of embedded ADC performance in a standard digital CMOS technology and to advance the achievable performance by solving the problems caused by mixed-signal integration. Targeted specifications are 50 Msamples/s, resolution up to 10 bit and maximum

effective resolution bandwidth with low power consumption.

In order to use the technology scaling of CMOS processes more and more functionality, both analog and digital, has to be integrated in CMOS. By solving the noise coupling problems with appropriate design techniques and by using efficient mixed-signal test methodologies, future products will benefit from smaller size, better reliability, lower cost and higher integration, eventually leading to systems on a chip (SOCs). The BANDIT project focuses on embedding a high-speed wideband ADC on a large digital telecom ASIC for WLAN applications. However a number of the methodologies being investigated in this project are more generally applicable to the integration of other analog blocks of mixed-signal receivers (as well as transmitters) or even mixed-signal ASICs in application domains other than telecom.

The main objectives for the project are:

- Simulation/analysis methodology for noise coupling,
- Design techniques/guidelines for digital low-noise circuits, for analog circuits and ADC architectures with reduced switching noise sensitivity,
- Design for test methodology for high-speed embedded ADCs.

Two versions of a demonstrator test chip will be designed and tested. The first version will contain an existing implementation of a high-speed ADC and a straightforward implementation of the digital multirate part. This first version of the demonstrator will allow us to test the ADC with the digital part switched either on or off. It will be possible to measure the performance degradation of the ADC due to digital switching noise, and to get in this way an indirect measure of the magnitude of the digital switching noise. The second version of the demonstrator chip will contain an improved version of the ADC which is less sensitive to substrate noise, and

an improved version of the digital multirate part which generates less noise.

Comparison of measurement results of both versions of the demonstrator will allow us to verify the achieved performance gain in the second version of the embedded high-speed ADC. We are mainly interested in the following ADC performance specifications: effective number of bits, effective resolution bandwidth and sampling rate. We can also directly compare the performance degradation due to switching noise in each version of the ADC. This will also give an indirect comparison of the amount of switching noise present in the two respective versions of the digital multirate part.

The measurement results obtained from both versions of the demonstrator ASICs can also be used as reference to evaluate the accuracy of the analysis/simulation methodology and models for noise coupling simulation.

2. SUBSTRATE MODELING

Substrate modeling can be done at several levels of detail [1]. The most complex models are based on complicated numerical extraction routines and take into account the different doping profiles of the substrate. The resulting substrate model consists of a 3-dimensional resistor mesh. Although these methods result in a very accurate substrate model, they are only applicable to small circuits because of the large number of circuit nodes extracted for the substrate.

The more simple models divide the substrate in one or two layers with a constant resistivity, depending on the type of substrate. When dealing with low-ohmic substrates with an epi layer the bulk is considered as one electrical node and the substrate resistances are defined by the epi layer. High-ohmic substrates must still be considered as two or three dimensional resistor meshes. For frequencies below 5-10 GHz the bulk silicon can be modeled by taking only resistive effects into account [2].

For low-ohmic substrate types the bulk can be considered as one electrical node. For this case the SPICE substrate model used for the simulations, is shown in figure 1, for the example of an inverter.

This substrate model is similar to the one presented in [3], except for the extra lateral resistances between bulk nodes and well contacts. The SPICE substrate model consists of the following elements: vertical coupling between substrate contacts and MOSFET bulk nodes to the common substrate, lateral coupling between MOSFET bulk nodes and the nearby well contacts and coupling capacitances from the nwell to the bulk. Element values can be estimated using contact geometry data, epi layer resistivity and nwell capacitance data.

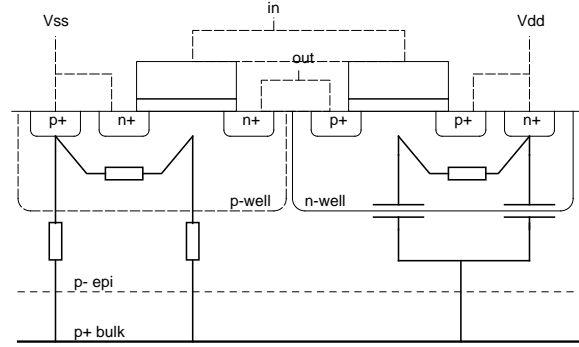


Figure 1: SPICE substrate model.

Accurate simulation of the substrate noise also requires that all package parasitics, such as bondwire inductances, are included in the SPICE model. This is important because substrate noise is not only caused by capacitive coupling from switching digital gates, but also by direct coupling from the noisy digital ground. Figure 2 shows the simulated substrate voltage caused by a 7-stage inverter chain. The plot on the left shows the substrate voltage in case of an ideal digital power supply. In this case all noise coupling is caused by the switching inverters. The plot on the right shows the case in which an inductance of 10 pH has been added in the digital power supply connection. In this situation the substrate noise is caused by coupling from the digital ground, and the waveform corresponds with the current drawn from the power supply.

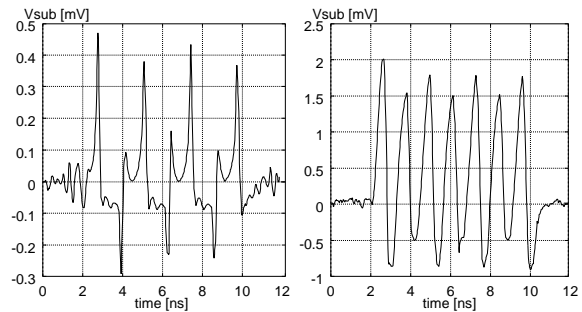


Figure 2: Substrate coupling originating from switching gates and from the digital ground.

For a simulation of substrate noise in a complete IC the substrate model must be combined with the SPICE description of the circuit and must also include package parasitics, such as bondwire inductance and resistance. But even such a simple SPICE substrate model will give rise to very long simulation times for complex digital systems. Therefore higher level models will be developed in the project, describing the substrate noise production of digital cells as function of the switching activity.

3. SUBSTRATE NOISE SIMULATIONS

Using the SPICE substrate model, described in the previous section, simulations can be performed of the substrate noise generated by relatively simple digital circuits. These simulations can be used to investigate the effect of different packaging techniques (wirebond, flipchip) on the substrate noise. Information about the time behavior of substrate noise can be useful to find quiet substrate noise timeslots to perform sensitive analog signal operations, such as sampling in a data converter. Similarly, in the frequency domain, quiet substrate noise frequency bands can be used to position the selected channels in communication transceivers.

An example of a time domain simulation of substrate noise can be seen in figure 3. Plotted in this figure is the voltage on the substrate noise caused by simultaneous switching of a number of flip-flops in a pseudo random generator. For this simulation the wirebond version contains 1 nH extra inductance in the power supply connection with respect to the flipchip version.

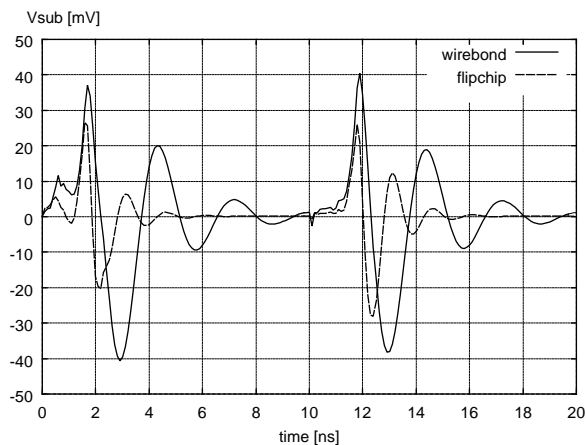


Figure 3: Substrate noise caused by switching of a pseudo-random generator.

Figure 3 clearly shows the influence of the extra inductance: the amplitude of the noise signal is increased and the duration of the ringing is increased. In both the flipchip and wirebond version the substrate noise is dominated by ringing from the digital power supply. This ringing is caused by the combination of inductance in the power supply connections and the circuit capacitance between power and ground on chip. The corresponding frequency spectra of the previous simulations are shown in figure 4.

The ringing of the substrate noise can easily be recognized in the frequency spectrum. For the wirebond version this ringing occurs around 300 MHz, for the flipchip version around 600 MHz.

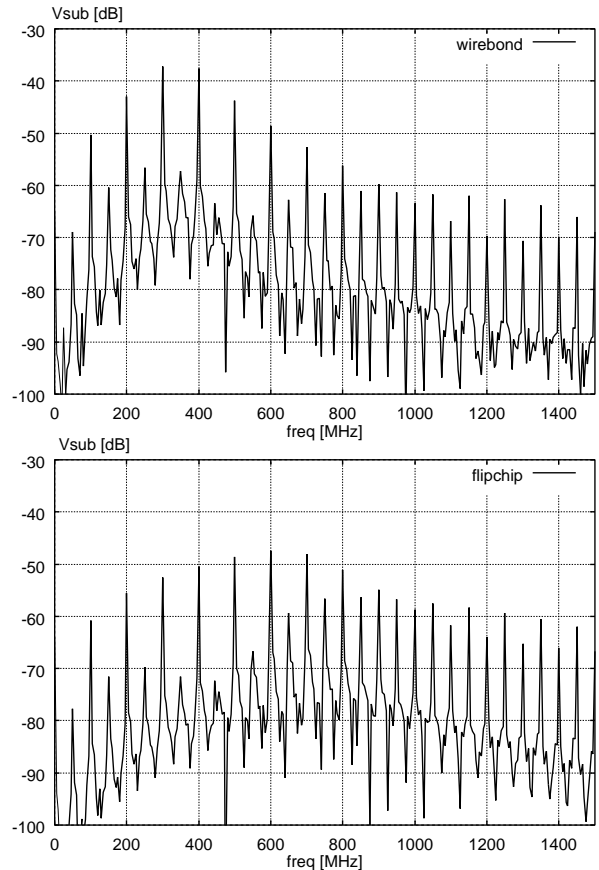


Figure 4: Frequency spectrum of substrate noise for wirebond and flipchip version.

It can also be seen that the maximal substrate noise amplitude, in the wirebond case, is larger than in the flipchip case. Apart from the ringing this simulation also shows that the difference between peak substrate noise levels, occurring at multiples of the clock frequency, are about 40 dB larger than the noise floor. This is important information when choosing frequency bands for analog signal operations.

Measurements on a test chip show a good agreement with the simulated substrate noise waveforms and spectra discussed above [4].

4. IMPACT OF SUBSTRATE NOISE ON PERFORMANCE OF ANALOG CIRCUITS

In mixed-signal ASICs, analog designers are confronted with the degradation of the performance of their circuits. The two main causes for this performance degradation are the coupling through the common substrate and the introduction of spikes, generated by the digital switching, in the power supply lines. In the particular case of an embedded ADC, some bits of accuracy can be lost due to this effect.

From an analog point of view the substrate coupling problem can be tackled in two ways. The first way is to reduce the substrate noise signal that can reach the analog part. This could be done, for example, by adding some protection structures around the analog part or by modifying the physical substrate properties themselves. The second way is to make the analog block insensitive, or at least less sensitive, to the substrate noise. Therefore, the development of simulations tools which take into account the substrate coupling and can estimate the degradations of the circuit, are extremely important.

In this project an ADC will be embedded in a noisy environment. For this design, we will analyze the effects of noise on some ADC topologies usable in our application. This analysis will be made by comparison between simulated results, including the substrate coupling effects, and measurements performed on the ADC. In this way, the sensitive point of our ADC will be identified, and the efficiency of the substrate analysis tools now available will be assessed.

At the same time, we will develop some test structures in a digital CMOS technology. In these test chips, we are interested in the analysis of the sensitive points in complex analog topologies (amplifiers, ADC, etc...) in order to be able to design topologies that are less sensitive to substrate noise. The generalization of designs based on fully differential structures [5], where all the on-chip signals are referred to an on-chip ground different from the off-chip ground, can be used to reduce the analog design sensitivity to the spikes on the power supply lines introduced by the digital switching. Nevertheless, this technique will require the implementation of on-chip adaptation structures to make the bridge between the on-chip and the off-chip worlds.

Mixed-mode designs also require the use of careful layout techniques. The use of guard rings around the analog structures can be used, if they are correctly placed and biased. The biasing requires the use of extra dedicated bonding pads with an applied potential different from the noisy digital ground, which would increase the noise injected in the substrate. The usefulness of these layout techniques depends largely on the type of substrate that is used. For a low-ohmic, epi-type substrate layout techniques to reduce substrate noise coupling are much less effective than for a high-ohmic substrate.

5. REFERENCES

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