



# Design Experiments for Measurement and Modeling of Digital Substrate Noise Generation

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# Project partners

## IWT project **FRONTENDS**

- Alcatel Microelectronics
- K.U. Leuven
- IMEC

## ESPRIT project **BANDIT**

- IMEC
- K.U. Leuven
- Ericsson Radio Systems

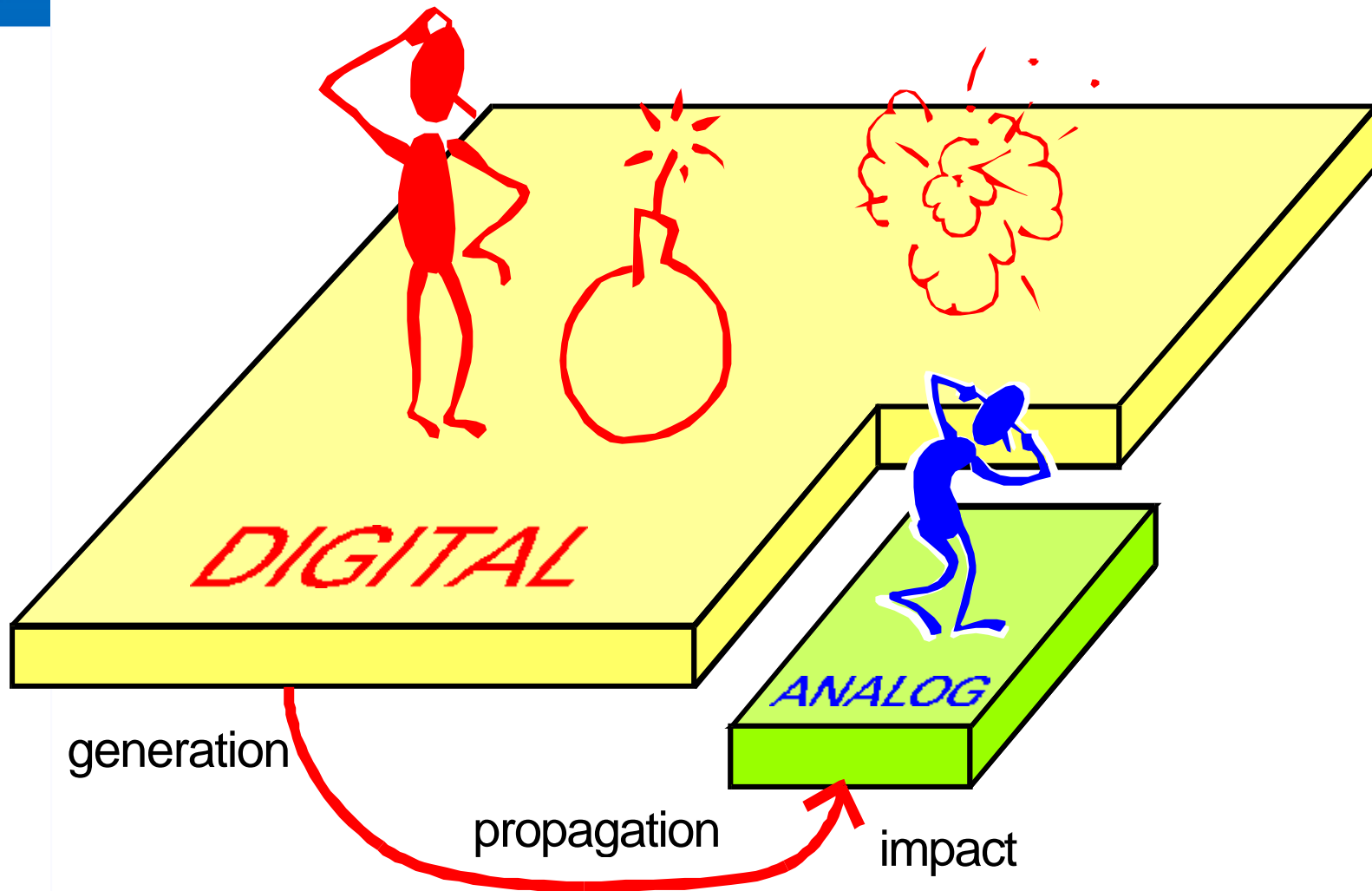


# Outline

- **Motivation**
- Introduction Substrate Noise Generation
- low-level (SPICE) modeling and measurements
- Conclusions



Goal: simulate substrate noise generation of large digital circuits





## Approach:

- Find simple but accurate SPICE substrate models for digital standard cells
- Verify the SPICE substrate noise simulations with measurements
- Develop a high-level substrate noise simulation methodology, based on the SPICE models
- At first, for low-ohmic epi-type substrates (Alcatel Microelectronics 0.5  $\mu\text{m}$  CMOS)

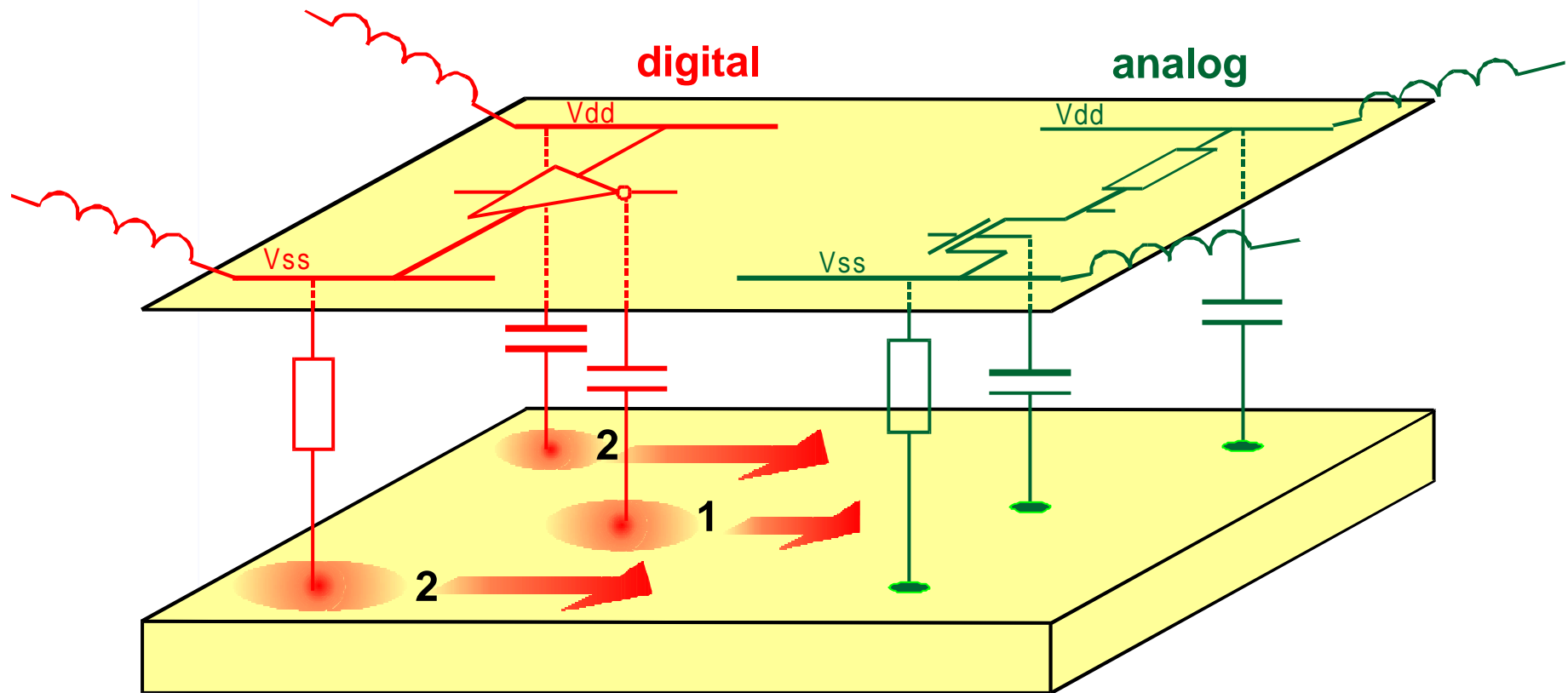


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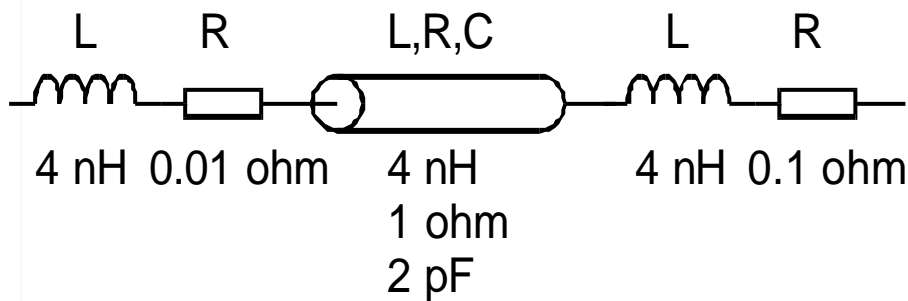
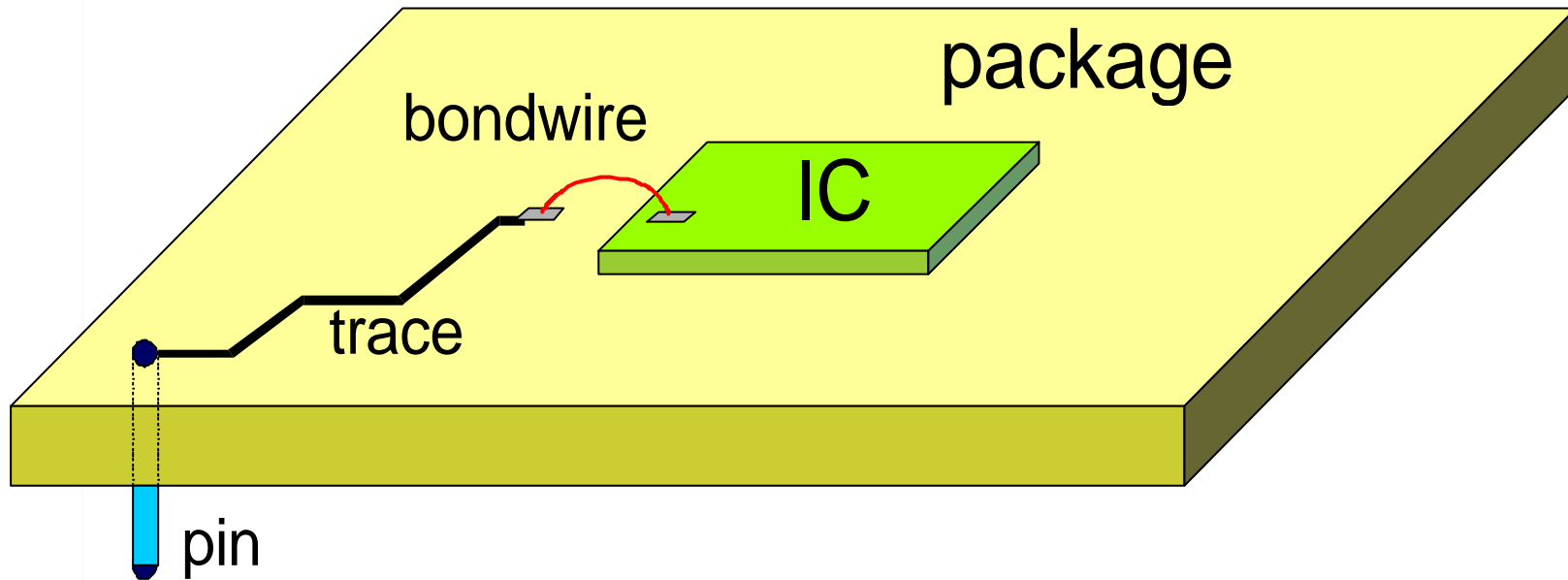


# Two sources of substrate noise: switching gates and the power supply





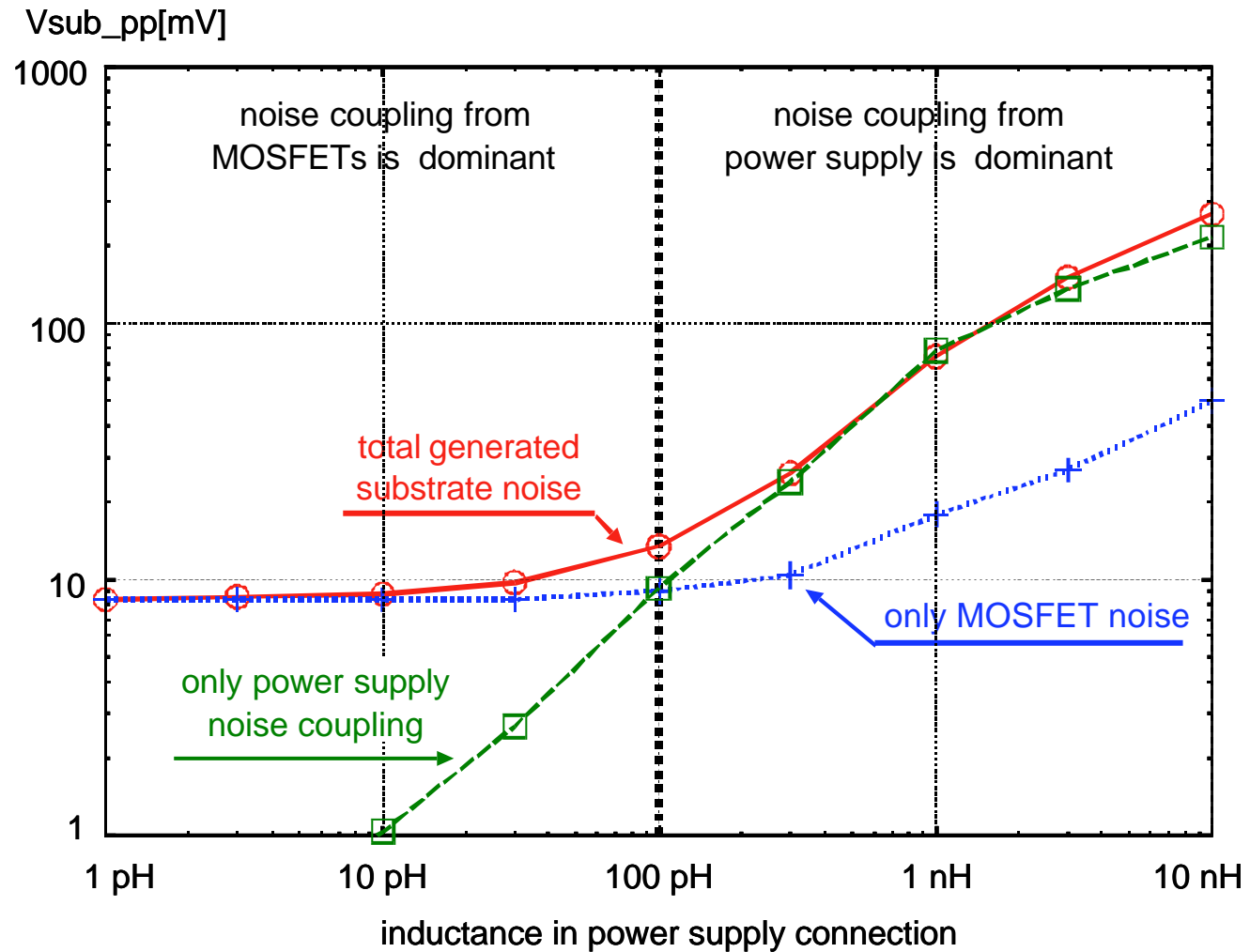
# External parasitics create power supply noise



1 Ghz => Z = 75 ohm



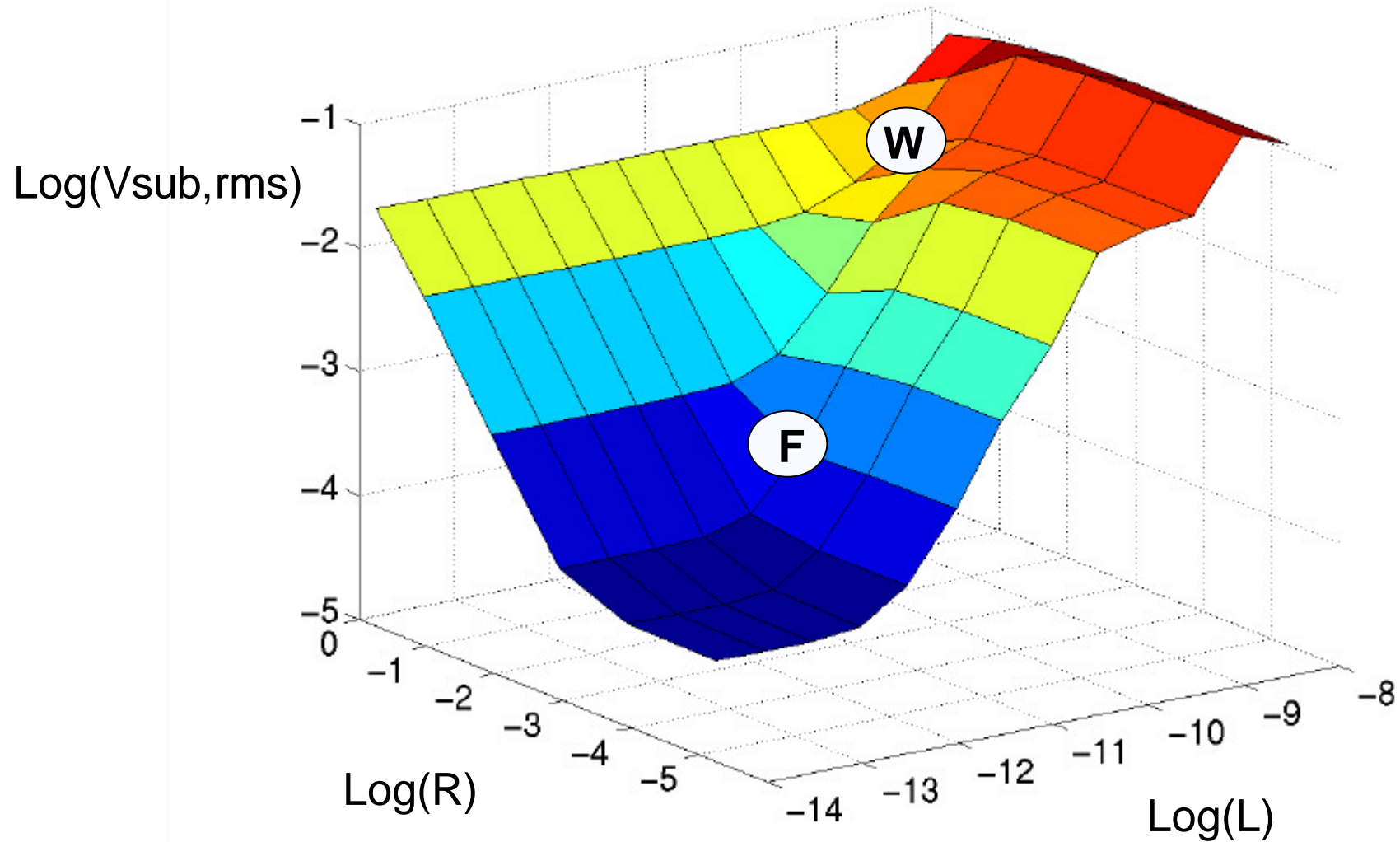
# Dominant noise source is determined by the external parasitics





# Substrate noise versus package parasitics

## Wirebond and Flipchip implementation



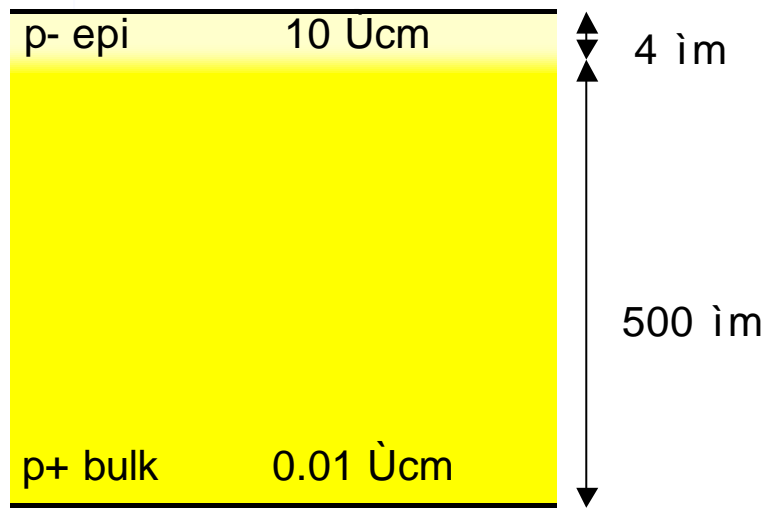


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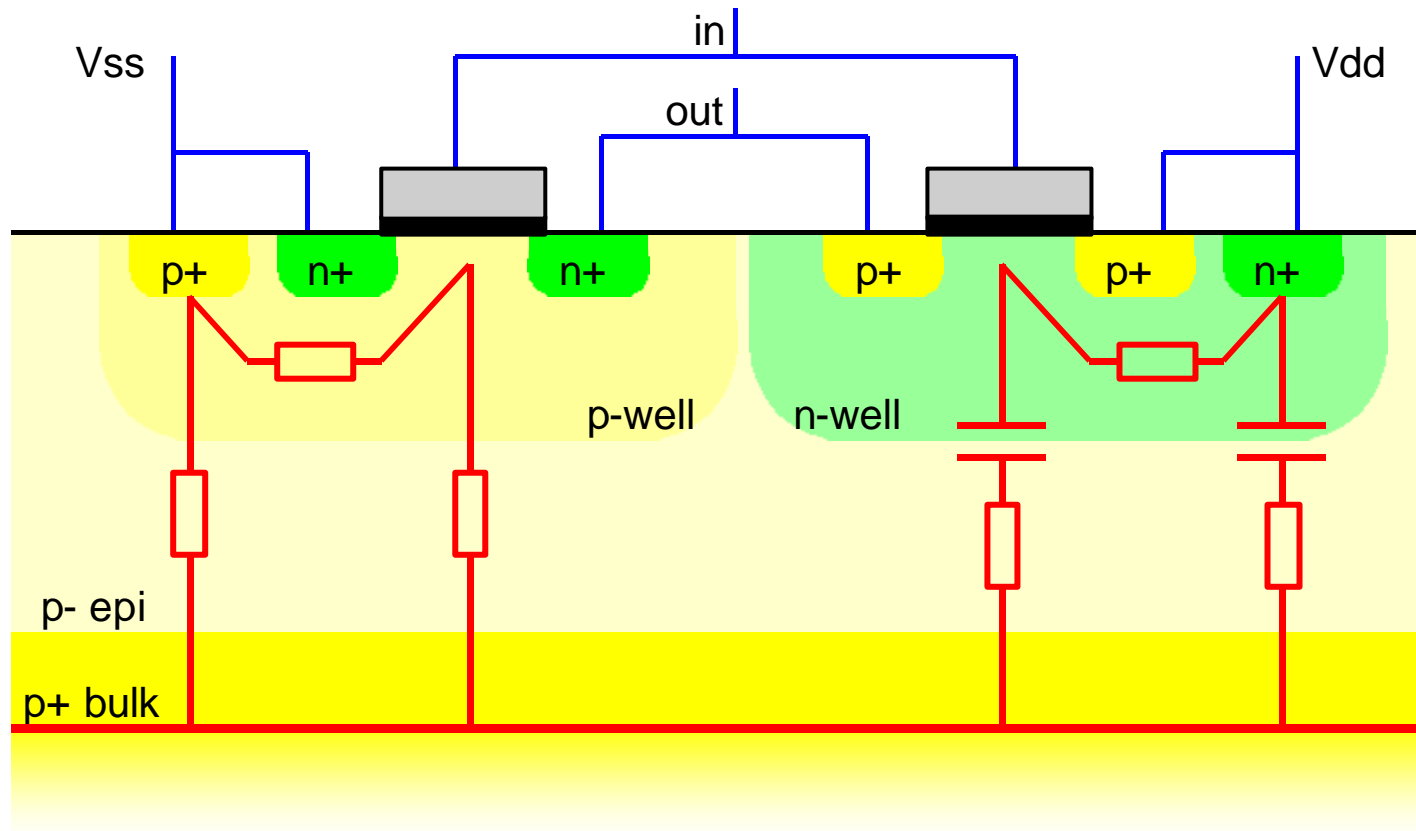
# Epi-type substrate can be approximated by one electrical substrate bulk node



epi type substrate  
low-ohmic bulk  
↓  
1 electrical node

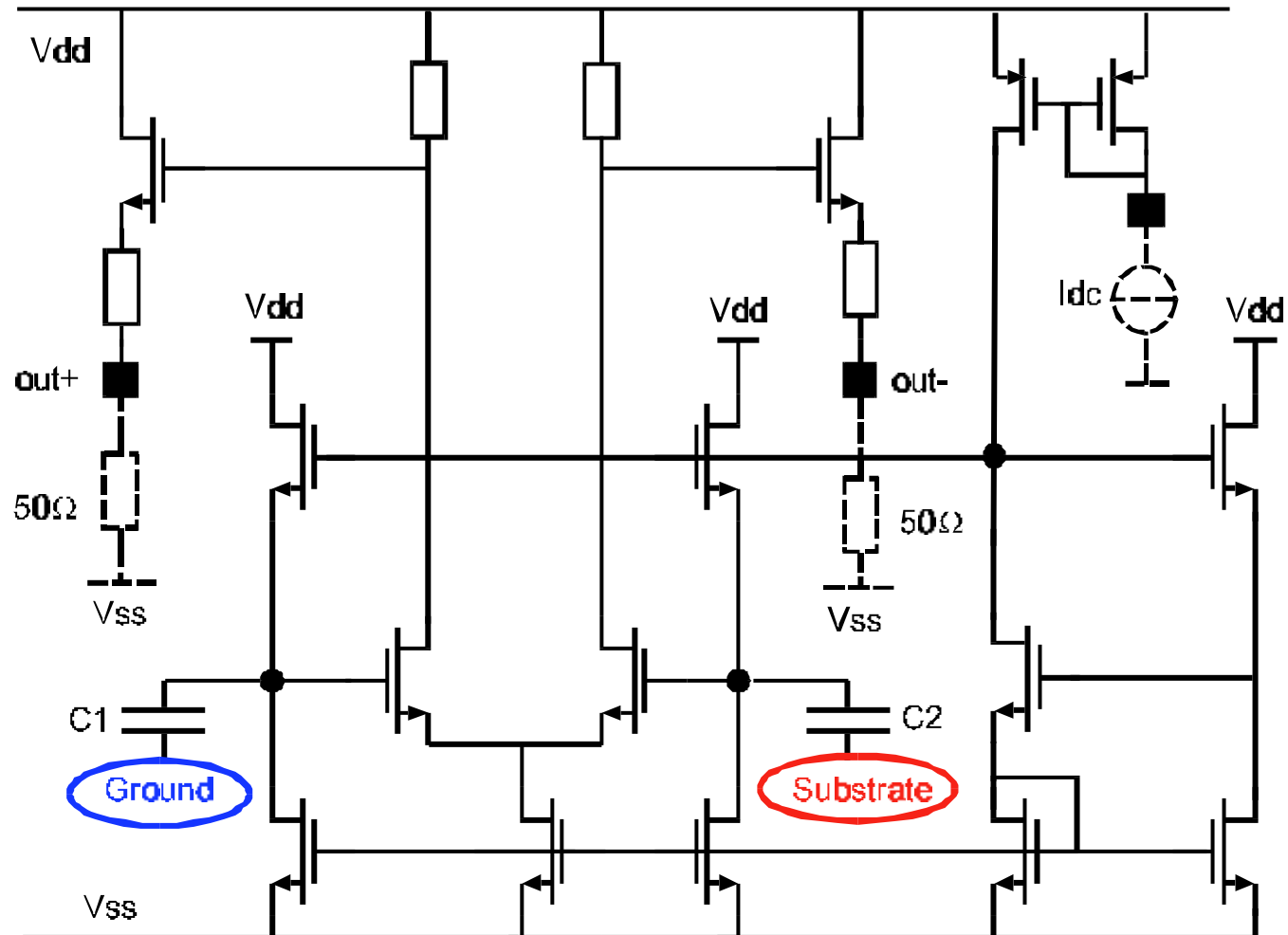


# Low-level (SPICE) substrate model



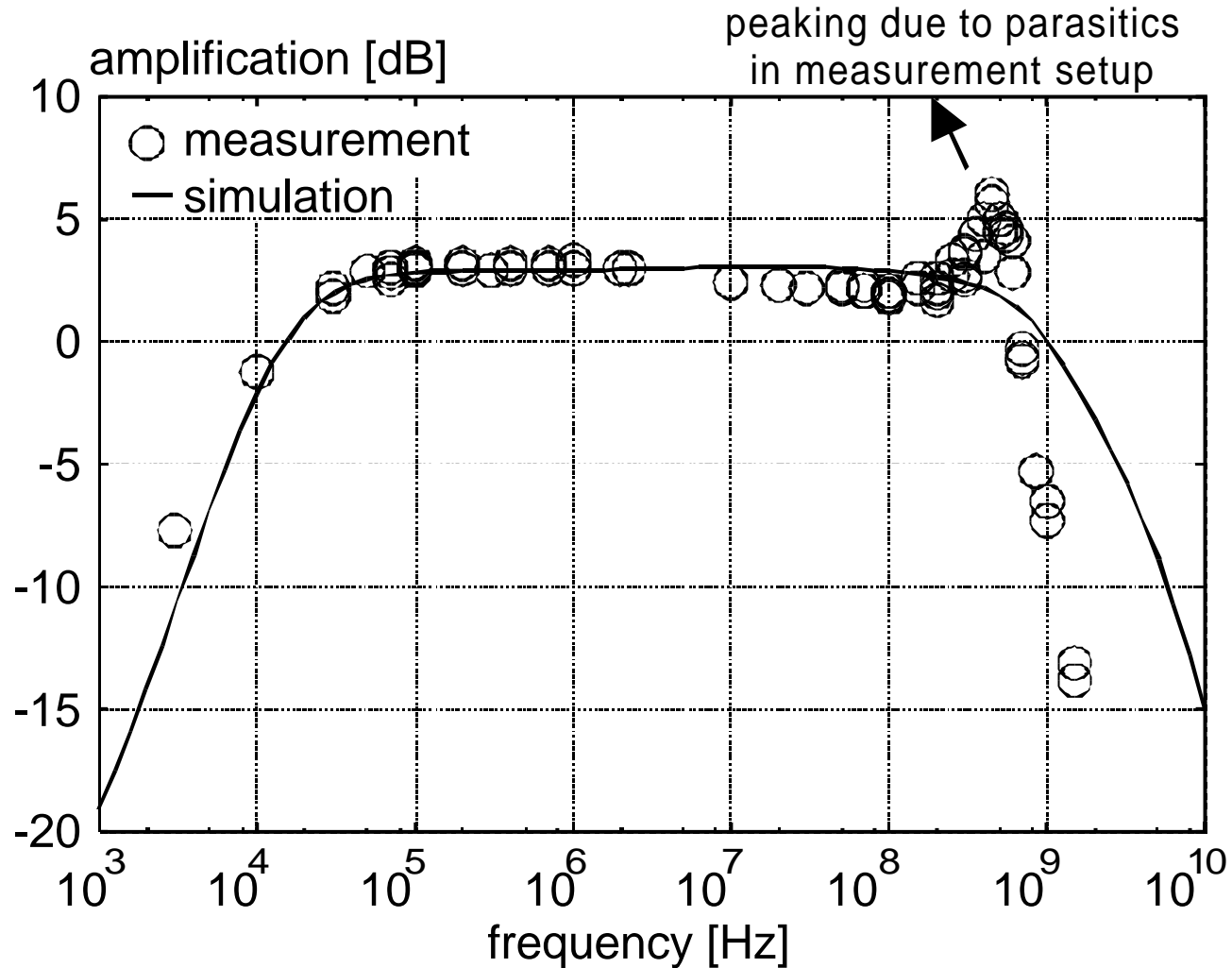


# Active substrate noise sensor to directly measure the substrate voltage





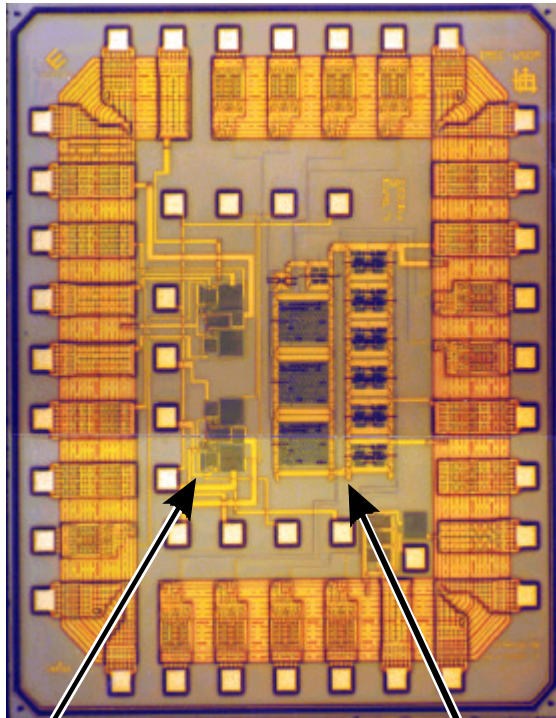
# Transfer function of the noise sensor





# Experimental ASICs to verify the low-level SPICE substrate models

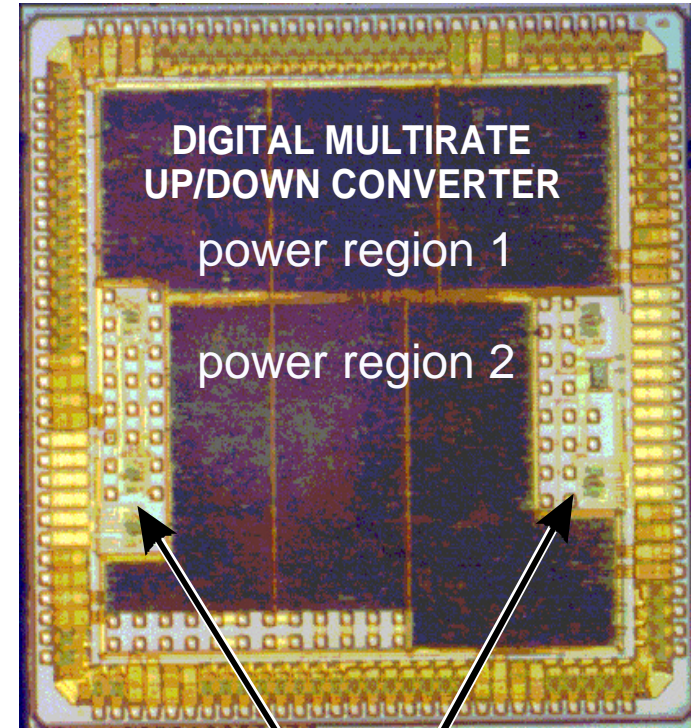
AuE 0.5um CMOS, 3.3 V  
test chip with noise generators



ANALOG  
NOISE  
SENSORS

DIGITAL  
NOISE  
GENERATORS

AuE 0.5um CMOS, 3.3V  
86kgate ASIC



DIGITAL MULTIRATE  
UP/DOWN CONVERTER

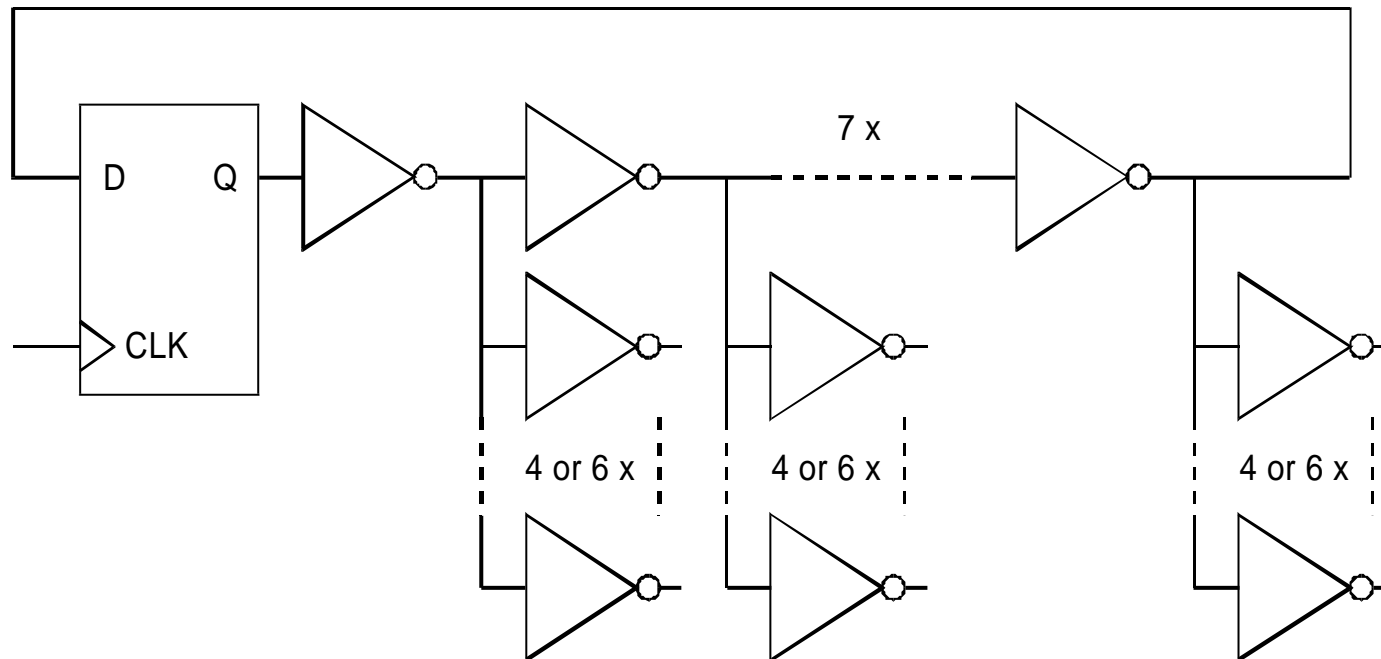
power region 1

power region 2

ANALOG  
NOISE SENSORS



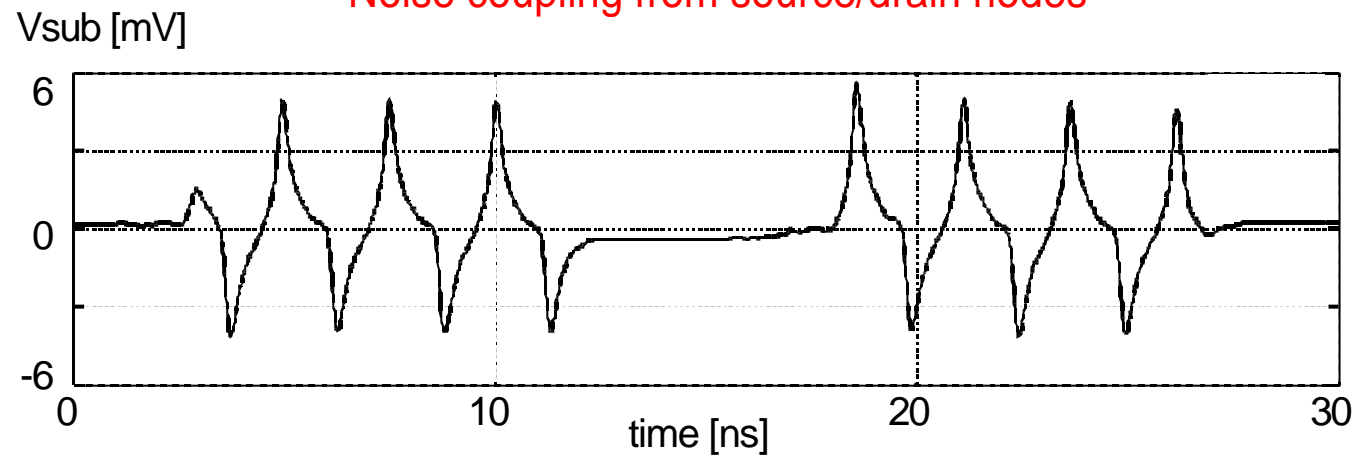
# Clocked ring oscillator used for substrate noise generation



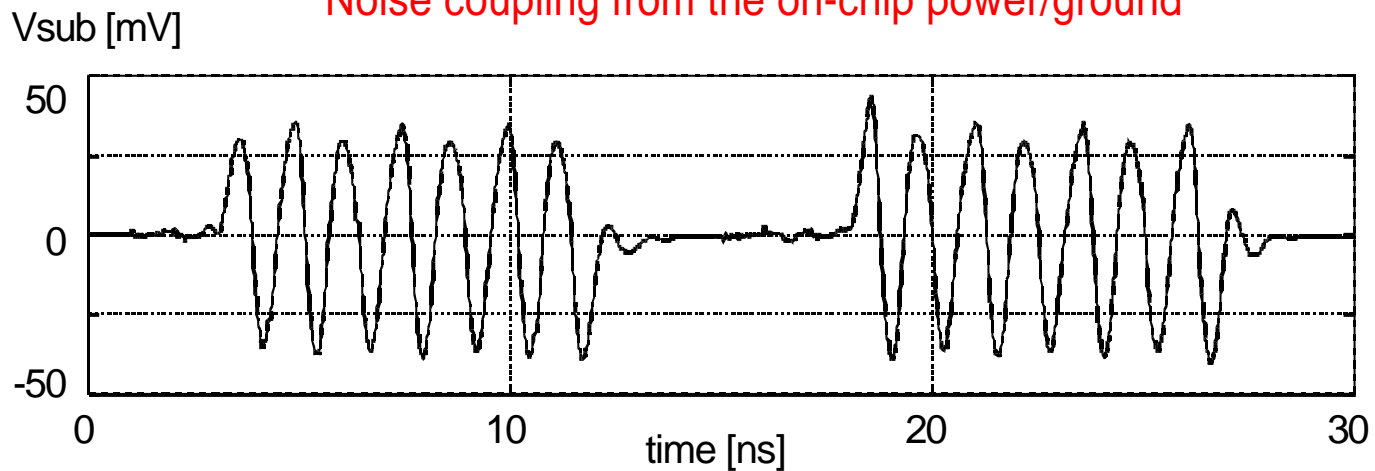


# Dominant substrate noise source determines the noise waveform

Noise coupling from source/drain nodes

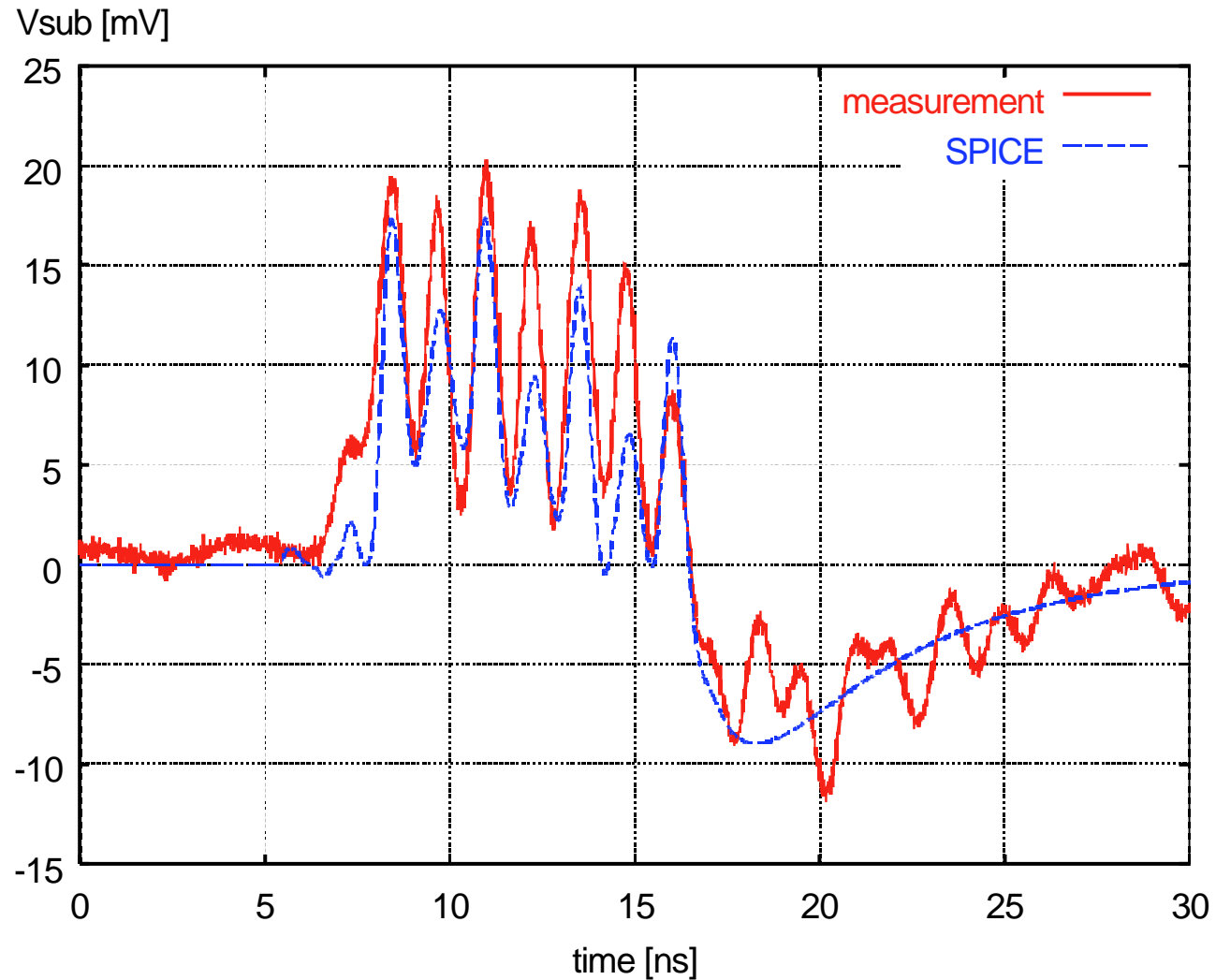


Noise coupling from the on-chip power/ground



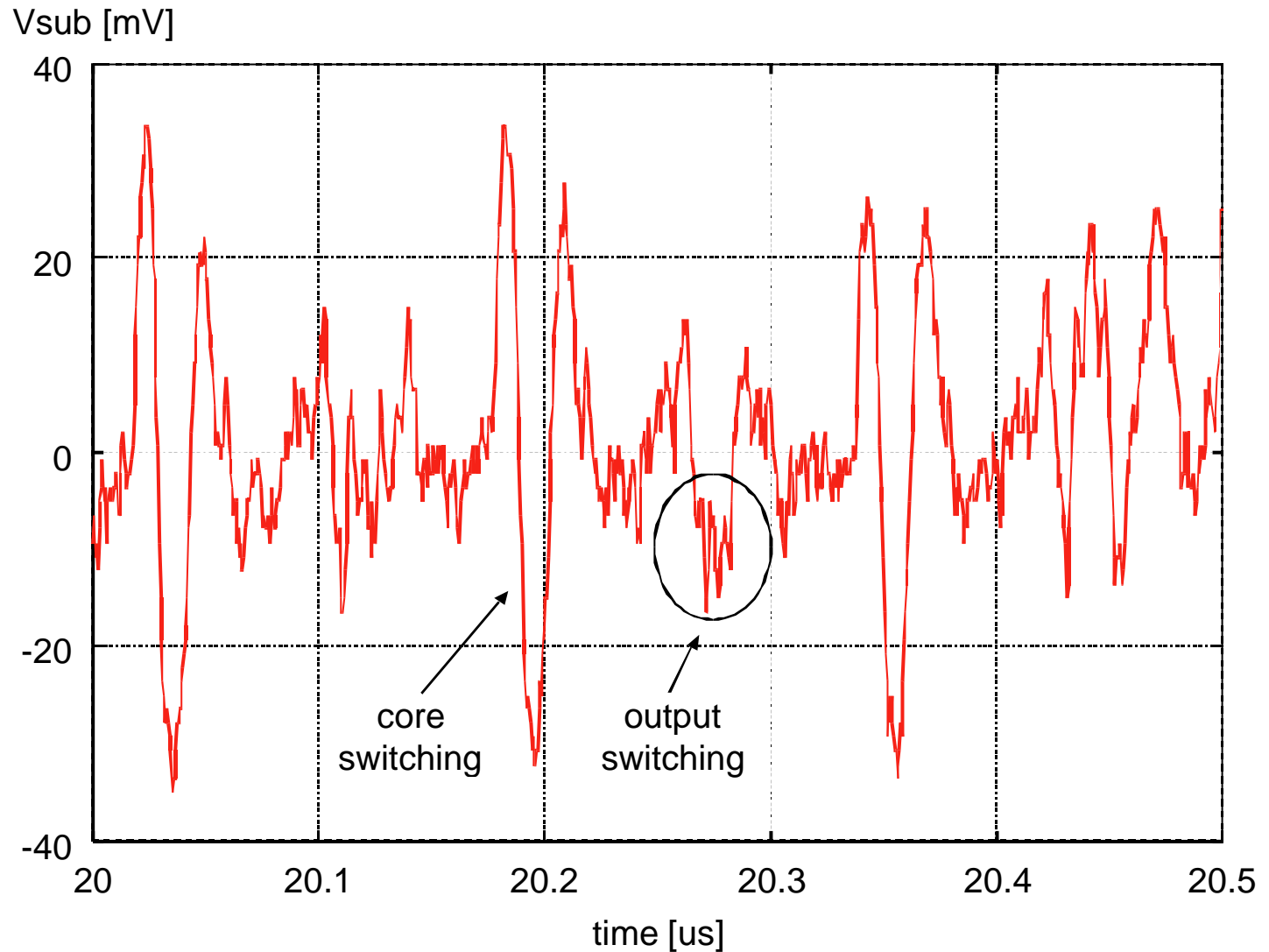


# Good agreement between measured and simulated substrate noise



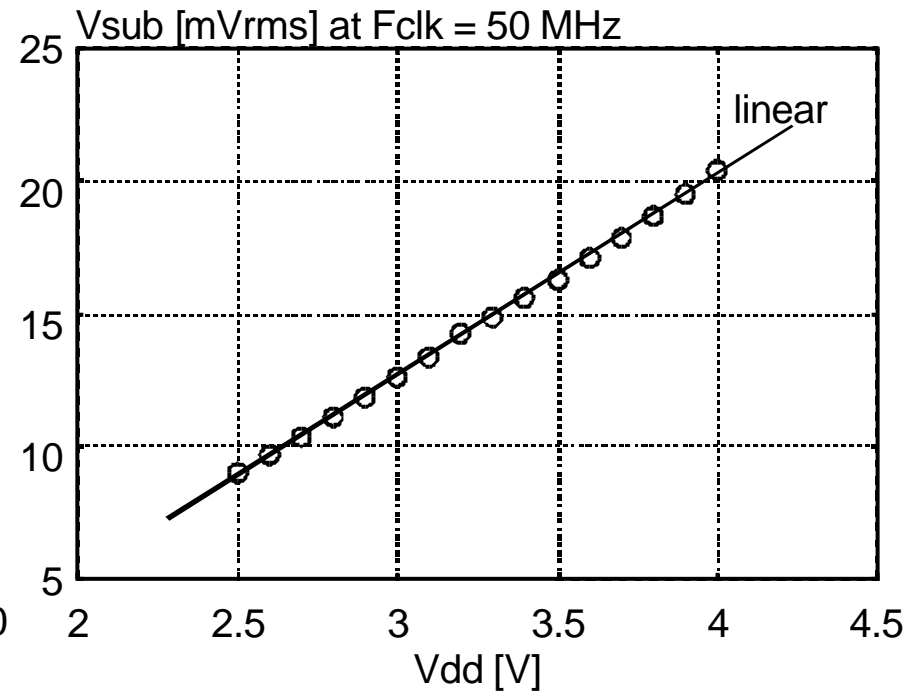
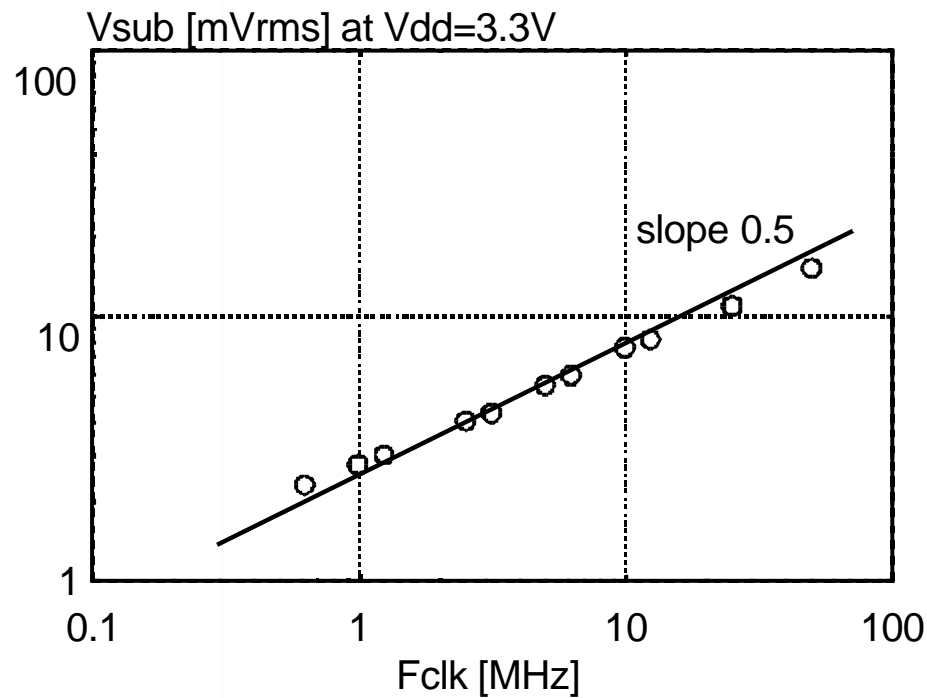


>80% of noise power is generated by simultaneous switching of core cells



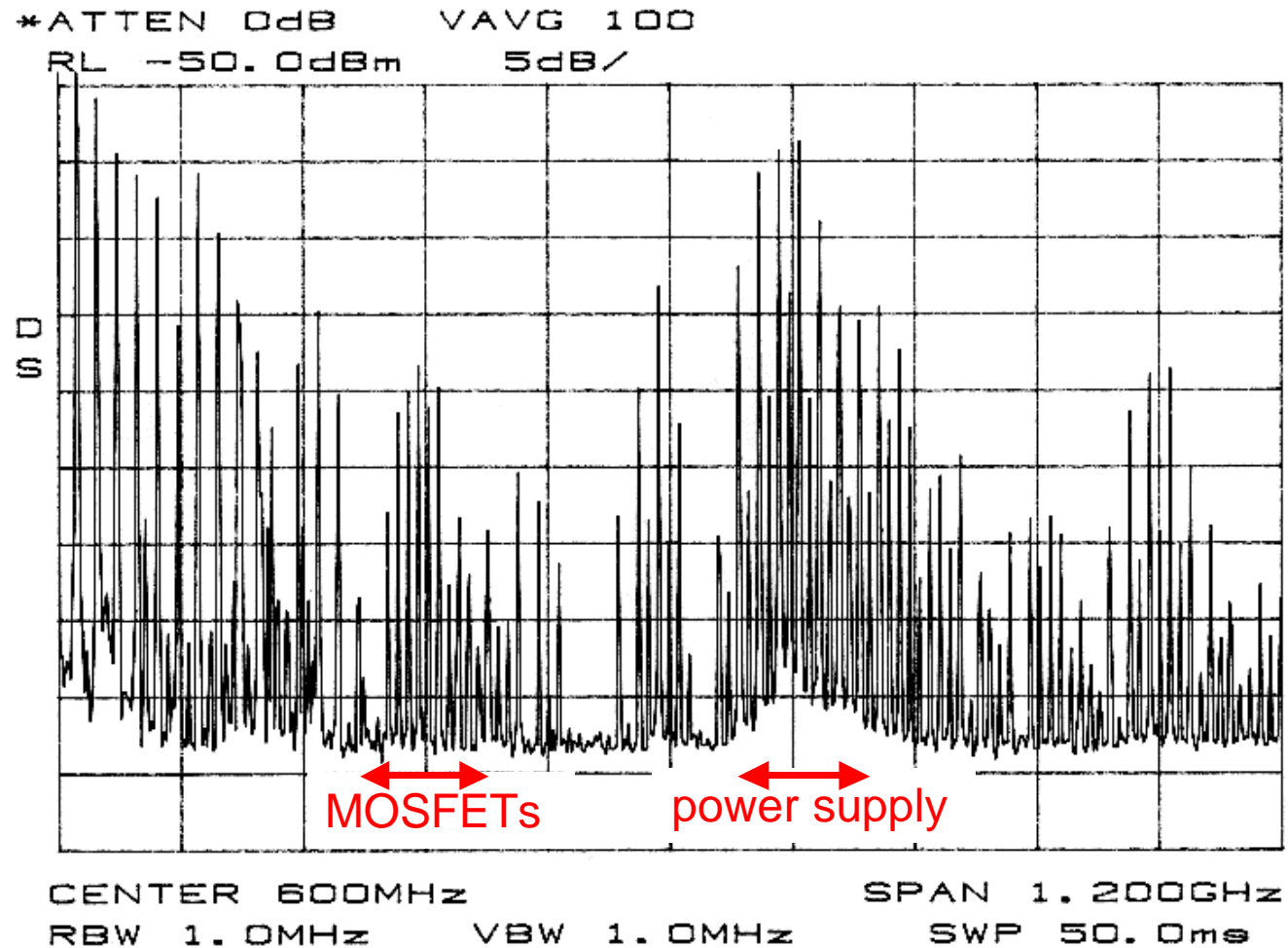


# Substrate noise power scales as CMOS power consumption : $V_{sub}^2 \sim f V_{dd}^2$



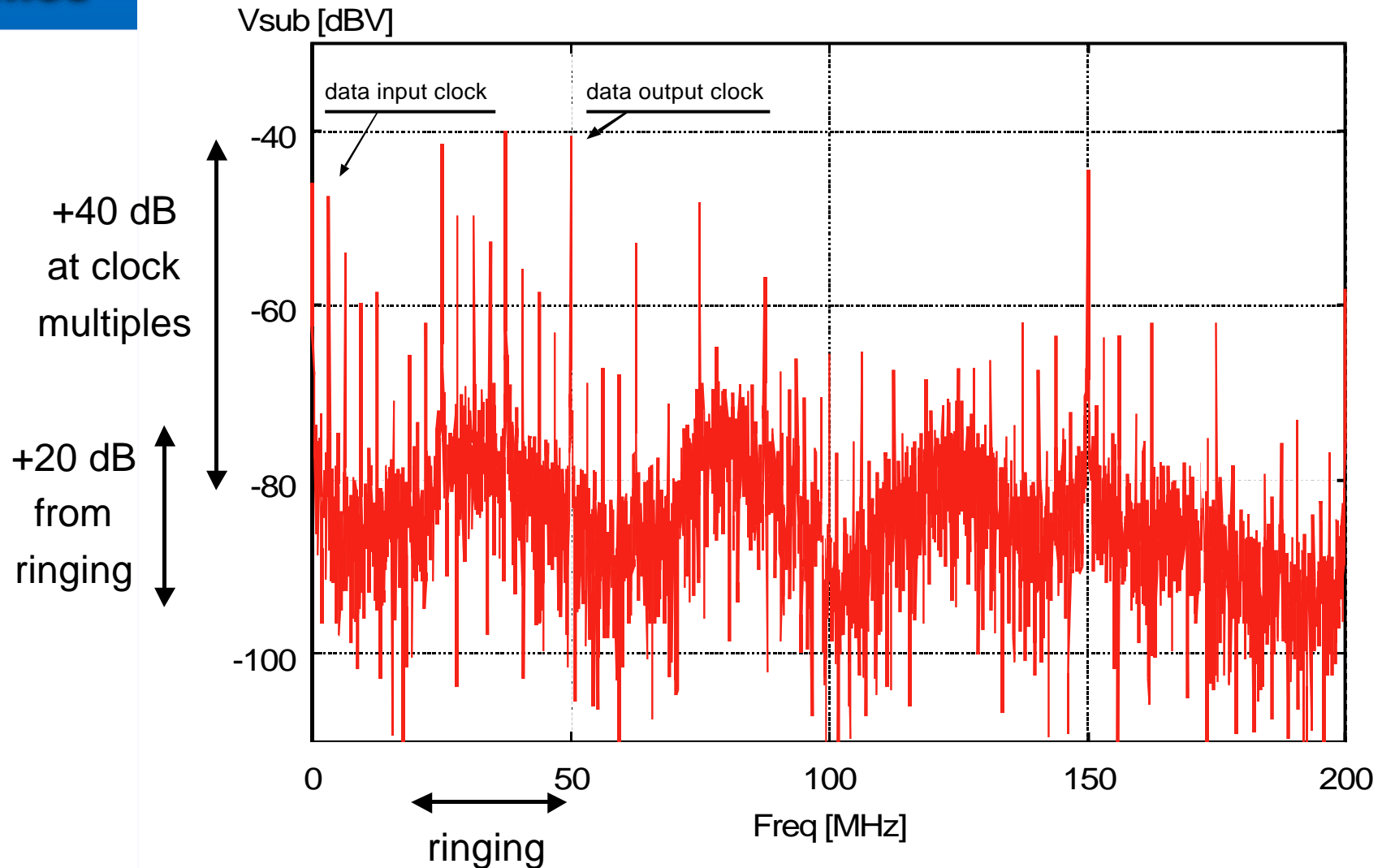


# Frequency spectrum of generated substrate noise





# Increase of substrate noise at clock multiples and due to ringing





## Conclusions from the measurements

- in most practical cases, substrate noise is caused by power supply noise coupling
- simultaneous switching of core cells (mostly flip-flops) generate more noise than IO buffers
- ringing of the power supply will increase the substrate noise
- in the frequency domain, substrate noise is concentrated at multiples of the digital clock frequency, with peaks up to 40 dB above the substrate noise floor



## Conclusions on modeling

- when modeling and simulating substrate noise generation all noise sources should be taken into account:
  - switching gates
  - power supply noise
  - package parasitics
- for epi-type substrates a simple SPICE substrate model can be used



# Related work and References

- Related work: High-level modeling and simulation of digital substrate noise generation
  - BANDIT project (see [HTTP://www.imec.be/bandit/](http://www.imec.be/bandit/))
- References:
  - M. van Heijningen, J. Compriet, P. Wambacq, S. Donnay, M. Engels, and I. Bolsens, "Analysis and Experimental Verification of Digital Substrate Noise Generation for Epi-Type Substrates," IEEE J. Solid-State Circuits, vol. 35, pp. 1002-1008, July 2000.
  - M. van Heijningen, M. Badaroglu, S. Donnay, M. Engels, and I. Bolsens, "High-Level Simulation of Substrate Noise Generation Including Power Supply Noise Coupling," in Proc. 37nd Design Automation Conference, pp. 446-451, 2000.
  - Y. Rolain, W. van Moer, G. Vandersteen, and M. van Heijningen, "Measuring mixed signal substrate coupling," in Proc. IMTC'2000, Baltimore, May, 2000.
  - M. van Heijningen, J. Compriet, P. Wambacq, S. Donnay, M. Engels, and I. Bolsens, "Modeling of Digital Substrate Noise Generation and Experimental Verification Using a Novel Substrate Noise Sensor," in Proceedings of the ESSCIRC, pp. 186-189, 1999.
  - M. van Heijningen, J. Compriet, P. Wambacq, S. Donnay, and I. Bolsens, "A Design Experiment for Measurement of the Spectral Content of Substrate Noise in Mixed-Signal Integrated Circuits," in Proc. 1999 Southwest Symposium on Mixed-Signal Design, April 11-13, Tucson AZ, USA, pp. 27-32, 1999.