Modeling of Digital Substrate Noise Generation and Experimental Verification Using a Novel Substrate Noise Sensor

Marc van Heijningen, John Compiet, Piet Wambacq, Stéphane Donnay,
Marc Engels and Ivo Bolsens
IMEC - DESICS
Kapeldreef 75
B-3001 Leuven, Belgium
Marc.VanHeijningen@imec.be

Abstract

Substrate coupling in mixed-signal ASICs can cause important performance degradation of the analog circuits. Accurate simulation is therefore needed to investigate the generation, propagation and impact of substrate noise. Recent studies have mainly concentrated on the time domain behavior of generated substrate noise and dealt mostly with noise injection from a single noise source. This paper will focus on the generation of substrate noise by digital circuits and on the spectral content of this noise. To simulate the noise generation a SPICE substrate model has been developed, which allows accurate simulation of substrate noise generated by small digital circuits. The correctness of this model has been verified with measurements of substrate noise on a test chip, using a novel wide-band, continuous-time substrate noise sensor, which allows accurate measurement of the spectral content of substrate noise. It is shown that the difference between spectral noise peaks and the noise floor can be up to 40 dB.

1. Introduction

Substrate coupling in mixed-signal ICs has been identified as a major problem. Nowadays substrate coupling becomes increasingly important due to the trend to integrate as much circuits as possible on the same die. Accurate simulation of the substrate voltage is necessary to analyze the proper functioning of analog circuits that are integrated on the same substrate as a digital circuit [1]. These simulations give insight in the time and frequency domain behavior of substrate noise. This information is very useful when designing mixed-signal ASICs: low substrate noise periods and frequency bands can be identified and used for sensitive analog signal operations.

In recent years a lot of research has been done on modeling the substrate and on substrate coupling reduction techniques [2] [3] [4]. Most publications deal with modeling and simulation of substrate noise or with measurements on small test structures, often using indirect measurement techniques. They also concentrate mostly on the time domain behavior of substrate noise.

In this paper a substrate modeling strategy is presented which allows accurate simulation of the time and frequency domain behavior of substrate noise generated by small digital circuits. To verify these simulations a test chip has been designed, containing a novel substrate noise sensor, which allows continuous-time, wide-band measurement of substrate noise. Measurements and simulations in the time and frequency domain will be presented.

2. Substrate modeling and noise coupling mechanisms

To simulate substrate noise a model of the substrate is necessary. Several techniques exist to determine such a model. These techniques vary from complicated electromagnetic models to simple lumped element models. The electro-magnetic techniques results in accurate models but are only applicable for small circuits because of the large number of substrate nodes that are created [3]. For low-ohmic (highly doped) substrates the bulk can be considered as one electrical node and only the resistance of the epi layer has to be taken into account [2]. This results in a simple lumped element model. Our test chip has been processed in a 0.5 μm CMOS twin well technology with a low-ohmic, epi-type substrate, and a single node substrate model will be used for the simulations.

This model is based on the model presented in [2], but lateral resistances between MOSFET bulk nodes and nearby well contact have been added. These lateral resistances are important, because they will reduce coupling from digital nodes and at the same time increase coupling from the power supply to the substrate. This is especially the case in twin-well technologies, which have nwells and pwells that are more highly doped than the epi layer. The SPICE substrate model used for the simulations is shown in figure 1, for the example of an inverter. The vertical resistances in the SPICE substrate model are calculated using the approximate expression [2] $R_{epi} \approx \frac{\rho_{epi}\, t_{epi}}{A} // \frac{\rho_{epi}}{P}$ with ρ_{epi} and t_{epi} the resistivity and thickness of the epi layer and A and P the area and perimeter of the substrate contact or MOSFET gate. The lateral resistances between well contacts and MOSFET bulk nodes are estimated us-

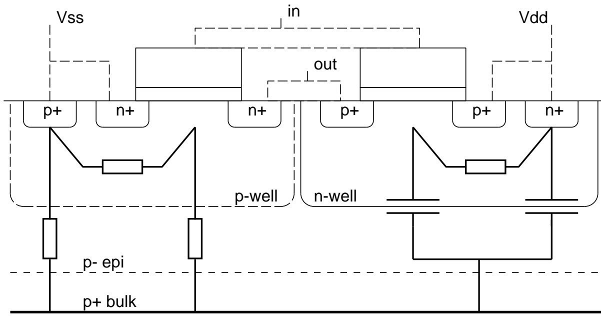

Figure 1. SPICE substrate model

ing the well sheet resistance. Nwell junction capacitances are calculated using technology data and the well geometry.

Although this is a simple model it can only be used for relatively small circuits, since the entire circuit must be simulated with SPICE. For an accurate simulation also the inductance of the power supply connections to the chip must be taken into account, because the noise on the digital power supply can easily dominate the substrate noise.

The impedance in the power supply connection determines which source of substrate noise will be dominant. In case of a very low supply impedance the dominant source of substrate noise will be capacitive coupling from switching digital nodes. But a soon as the supply impedance becomes larger, and di/dt noise on the digital ground gets larger than the capacitive coupling noise, the dominant source of substrate noise is coupling from the digital ground via the low resistive substrate connections.

A simulation of substrate noise coupling from a 7-stage inverter chain is shown on the left in figure 2. This simulation has been performed with no inductance in the power supply connection and shows 7 peaks (4 times up, 3 times down), corresponding with the 7 transitions on the output nodes of the inverters. When an inductance of 10 pH is added in the power supply connection substrate noise is dominated by coupling from this power supply. This is visible in figure 2 on the right. Now 7 noise peaks are visible, corresponding to the current drawn by the switching inverters from the power supply. It is clear that the spectral content of the substrate coupling will depend largely on the dominant type of coupling. In practical cases noise coupling from the power supply will be dominant, because of the low impedance between the digital ground and the substrate, and the spectral content of the substrate noise will be related to the current drawn from the power supply.

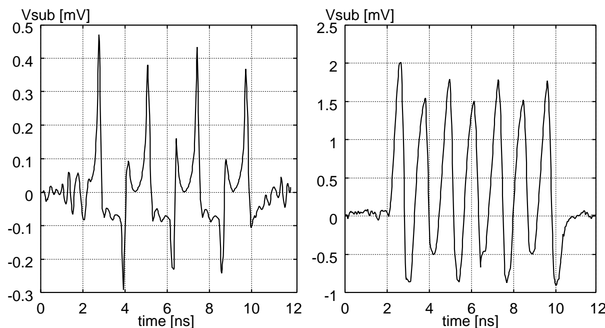

Figure 2. Simulated coupling from switching nodes (left) and from the power supply (right)

3. Substrate noise measurement techniques

Measurement of substrate noise is important to verify the correctness of modeling and simulations. This section will describe some existing measurement techniques and the problems associated with these techniques, followed by the description of our novel wide-band, continuous-time analog substrate noise amplifier.

3.1. Existing measurement techniques

A simple measurement technique, used in a number of publications, involves the use of the threshold voltage modulation of a single MOSFET [2] [5]. This is however an indirect measurement technique: not the substrate voltage is measured but the influence of the substrate voltage on the MOSFET current. The exact bulk transconductance must be known to calculate the substrate voltage. This method is also single-ended and thus sensitive to other noise sources and crosstalk. Also the bandwidth is not very high.

Another indirect measurement technique involves the use of voltage comparators as noise sensors [6]. With this method only the peak amplitudes and the rms voltage of the substrate noise are measured. The actual waveform cannot be measured.

A continuous-time, direct measurement technique is the use of an analog differential amplifier, with one input connected to the substrate and the other to a quiet reference signal [7] [8]. The sensor presented in [7] however, has only a limited bandwidth and measurement of actual coupling from switching digital nodes is not possible due to this bandwidth limitation. A differential sensor with a larger bandwidth is presented in [8] and will be described below.

3.2. Differential substrate noise amplifier

The substrate noise sensor, used in our experiments, is a differential amplifier with one input connected to a quiet ground and the other input connected to the substrate. Main objectives during the design have been a large bandwidth (over 500 MHz) and the ability to deliver a differential output signal in a 50 Ω load. The principle schematic of the sensor is shown in figure 3. The coupling capacitors C1 and C2 have been implemented as MOS capacitors. For the substrate voltage coupling capacitor, C2, source and drain have been connected to a substrate contact, surrounding the transistor. A measurement of the transfer function of this sensor is shown in figure 4. The solid curve shows a number of measurements and the dotted curve represents a SPICE simulation.

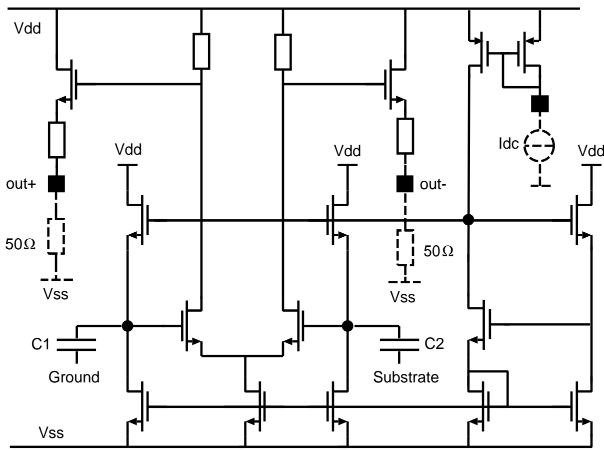

Figure 3. Noise Sensor Schematic

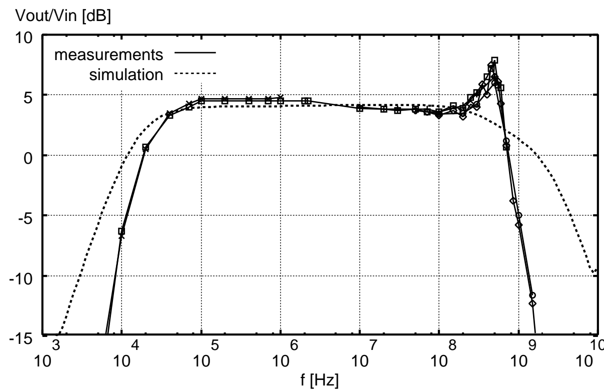

Figure 4. Noise Sensor Transfer Function

It can be seen that the bandwidth of the sensor is 200 kHz to 500 MHz, with an amplification between 3 and 4 dB. Peaking of the amplification around 500 MHz is probably due to inductances in the measurement setup. Differences between the simulation and the measurements at the low and high end of the bandwidth of the sensor are caused by external bias tees and a power combiner in the measurement setup, which have a bandwidth of 100 kHz to 1 GHz.

4. Experimental results

The measurements have been performed on an experimental test chip, which contains several digital circuits for the noise generation and a substrate noise sensor for the noise measurements. This chip has been mounted by a wirebond and flipchip technique onto a Multi Chip Module (MCM). The MCM is mounted on a Printed Circuit Board (PCB). Digital control signals are wirebonded from the PCB to the MCM. Clock signals, analog outputs and power supply are connected directly to the MCM via multi-contact wafer probes.

4.1. Time domain substrate noise

The substrate noise caused by a 7-stage inverter chain has been measured on a flipchip and a wirebond mounted version of the test chip. The measured noise for the two versions is shown in figure 5. The inverters in the chain

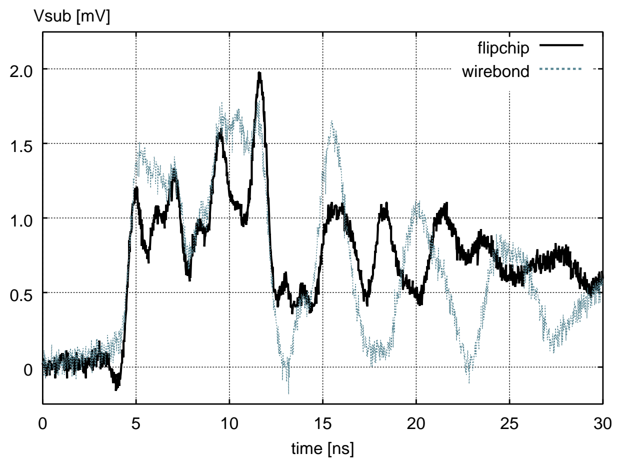

Figure 5. Measured substrate noise caused by switching a 7-stage inverter chain for a flipchip and wirebond version

are switching in the time period from 4 to 12 ns. During and after the switching ringing is coupled to the substrate from the digital supply. The measured switching noise on the flipchip version shows 7 edges, caused by coupling from the digital nodes. These individual edges are much less visible for the wirebond version. For this wirebond version the amplitude of the ringing is larger than for the flipchip version. The frequency of this ringing, which is around 200 MHz, is caused by the combination of the circuit capacitance (approximately 75 pF) and the total bondwire inductance (2x4 nH).

Figure 6 shows a comparison of a SPICE simulation and measurement for the wirebond version, again for switching noise from the 7-stage inverter chain. An inductance

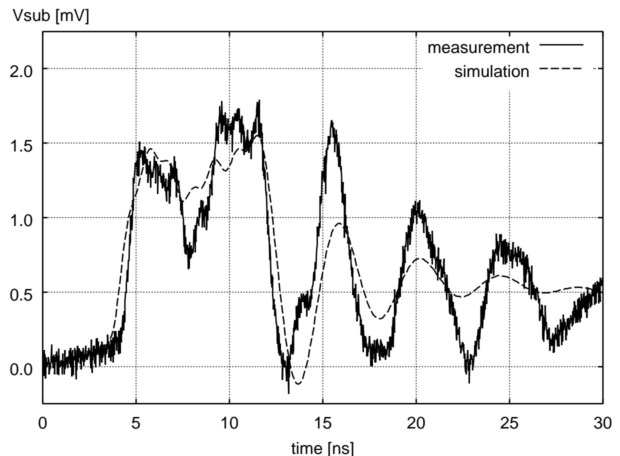

Figure 6. Measurement and simulation of substrate noise caused by switching a 7-stage inverter chain for a wirebond version

of 4 nH in the power supply connection has been added to model the bondwire connection. Also a capacitance from substrate to ground has been added to simulate the

capacitive effect of the floating substrate, which is probably causing the offset in the measured signal occuring after the switching. When these parasitics are taken into account, the simulation corresponds very well with the measurement.

4.2. Spectral content measurement

The frequency spectrum of the measured substrate noise has been obtained by taking an FFT of the time domain signal. The resulting spectrum is shown in figure 7. This figure shows the substrate voltage, relative to a 1 volt sine wave, caused by switching an inverter chain at 20 MHz. In this case the test chip has been wirebonded to investigate the influence of the power supply connection inductance. The increase of noise around 200 MHz is

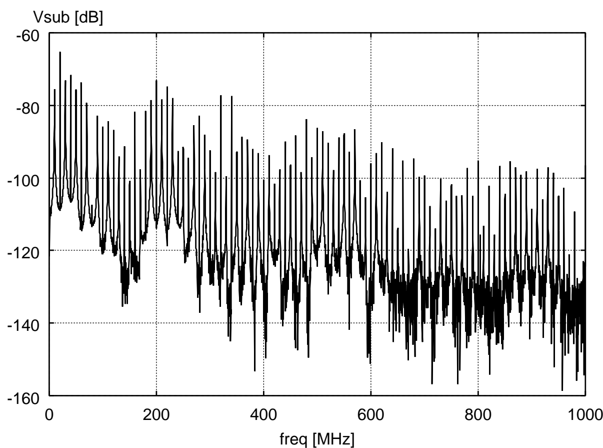

Figure 7. Frequency spectrum of measured substrate noise caused by switching a 7-stage inverter chain for a wirebonded chip version

caused by ringing of the power supply, which couples to the substrate. The inverters themselves switch at a frequency of around 900 MHz. This results in only a slight increase of the noise floor. Also visible in the figure is that the difference between peak noise levels and the noise floor is around 40 dB, which has also been observed in simulations. This is important information when designing mixed-signal ASICs and decisions have to be made about the placement of analog frequency channels.

From the previous measurement it can be concluded that substrate noise is concentrated at multiples of the digital clock frequency. In [9] however, it is concluded, based on high-level substrate noise simulations, that most substrate noise is concentrated around one frequency, corresponding with the inverse of the gate delay, and that this frequency is not related with the digital clock frequency. They have, however, only taken into account the coupling from digital switching nodes, and not noise coupling from the power supply. This indicates the importance of including power supply noise coupling to the substrate in the simulations.

5. Conclusions

The presented novel noise sensor has proven to be a valuable tool in the investigation of substrate noise. It allows continuous-time, wide-band measurements of substrate noise up to 1 GHz, which is necessary for determining the spectral content of substrate noise and checking the validity of the substrate model. The simulated substrate noise waveforms have shown good correspondence with the measurements, indicating the correctness of this model. Accurate simulations however, do require that all parasitics, especially in the power supply connections, must be taken into account. The measured spectrum of the substrate noise has shown that most substrate noise is concentrated at multiples of the digital clock and that ringing of the digital power supply dominates coupling from digital nodes. The measured difference between peak noise levels and the noise floor is 40 dB, indicating the importance of a good selection of digital clock frequency and analog IF frequencies (frequency planning) in integrated transceiver front-ends.

Acknowledgments

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References

[1] T. J. Schmerbeck, *Low-power HF microelectronics: a unified approach*, ch. 10: Noise coupling in mixed-signal ASICs. Institution of Electrical Engineers, 1996.

[2] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 28, pp. 420–430, Apr. 1993.

[3] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE J. Solid-State Circuits*, vol. 31, pp. 344–353, Mar. 1996.

[4] N. K. Verghese and D. J. Allstot, "Verification of rf and mixed-signal integrated circuits for substrate coupling effects," in *Proceedings of the Custom Integrated Circuits Conference*, pp. 363–370, 1997.

[5] T. Blalack, J. Lau, F. J. R. Clément, and B. A. Wooley, "Experimental results and modeling of noise coupling in a lightly doped substrate," in *Proc. IEEE 1996 IEDM*, pp. 623–626, Dec. 1996.

[6] K. Makie-Fukuda, T. Kikuchi, T. Matsuura, and M. Hotta, "Measurement of digital noise in mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 30, pp. 87–92, Feb. 1995.

[7] M. Nagata and A. Iwata, "Substrate noise simulation techniques for analog-digital mixed lsi design," *IEICE trans. fundamentals*, vol. E82-A, pp. 271–277, Feb. 1999.

[8] M. van Heijningen, J. Compiet, P. Wambacq, S. Donnay, and I. Bolsens, "A design experiment for measurement of the spectral content of substrate noise in mixed-signal integrated circuits," in *Proceedings of the 1999 Southwest Symposium on Mixed-Signal Design, April 11-13, Tucson AZ, USA*, 1999.

[9] P. Miliozzi, L. Carloni, E. Charbon, and A. Sangiovanni-Vincentelli, "Subwave: a methodology for modeling digital substrate noise injection in mixed-signal ics," in *Proceedings of the Custom Integrated Circuits Conference*, pp. 385–388, 1996.