Modeling of Substrate Noise Coupling in Digital ASICs with Embedded Analog-to-Digital Converters

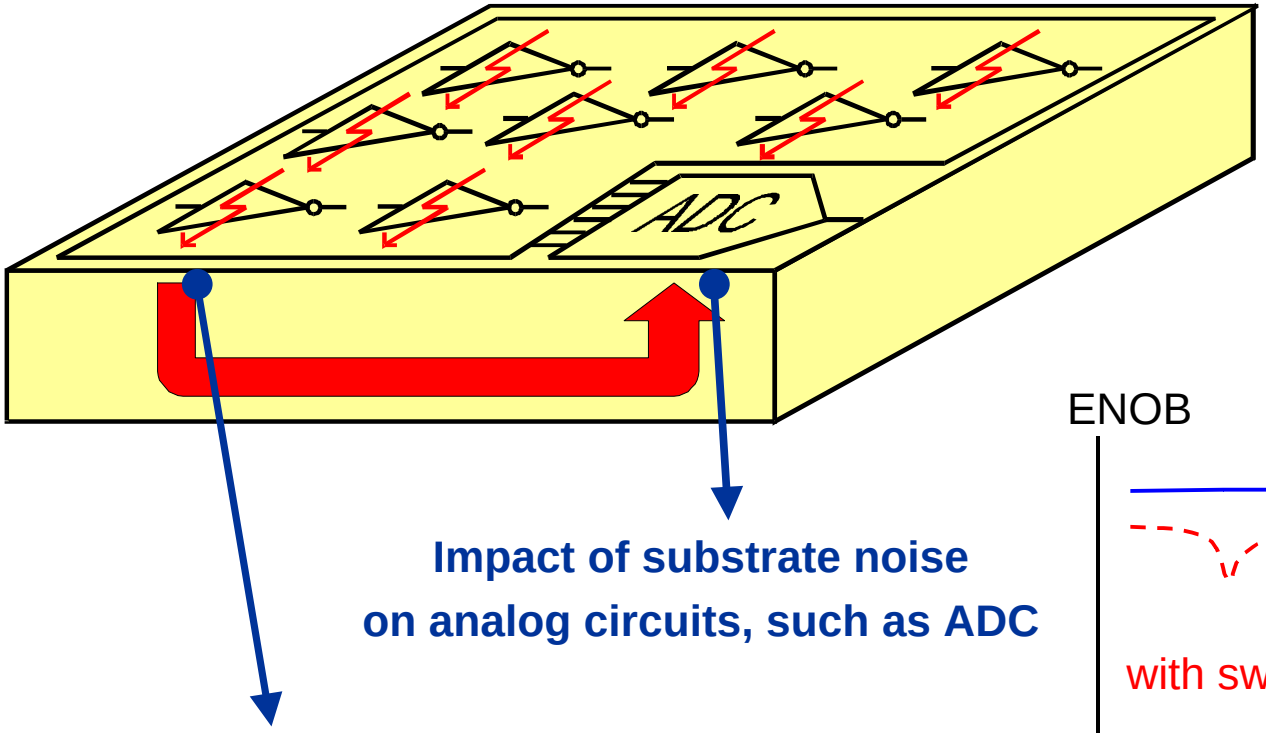
Mustafa Badaroglu, Marc van Heijningen, Stephane Donnay

IMEC - DESICS - MIRA, Leuven, Belgium

Yann Zinzius, Erik Lauwers, Georges Gielen, Willy Sansen

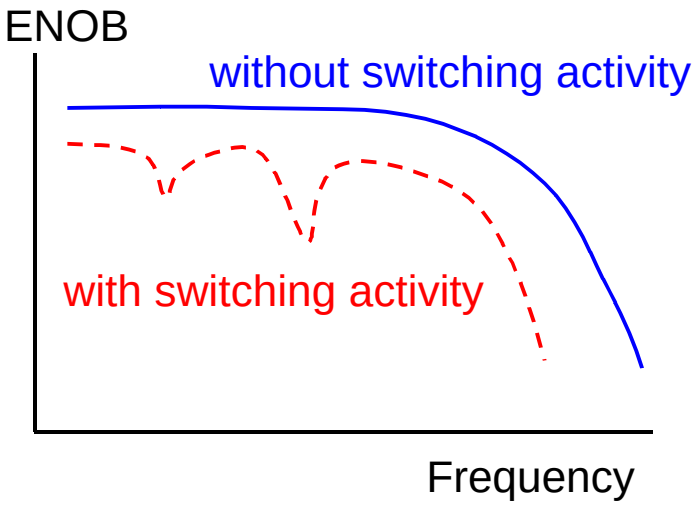
K. U. Leuven ESAT-MICAS, Belgium

Substrate noise coupling will degrade the performance of embedded analog circuits



Impact of substrate noise on analog circuits, such as ADC

Substrate noise generation by switching digital circuits



OUTLINE

1. High level modeling and simulation of digital noise generation

Mustafa Badaroglu, Marc van Heijningen, Stephane Donnay

IMEC - DESICS - MIRA, Leuven, Belgium

2. Evaluation of the substrate noise effect on analog circuits in mixed-signal designs

Yann Zinzius, Erik Lauwers, Georges Gielen, Willy Sansen

K.U. Leuven - ESAT - MICAS, Belgium

1. High level modeling and simulation of digital noise generation

Mustafa Badaroglu, Marc van Heijningen, Stephane Donnay

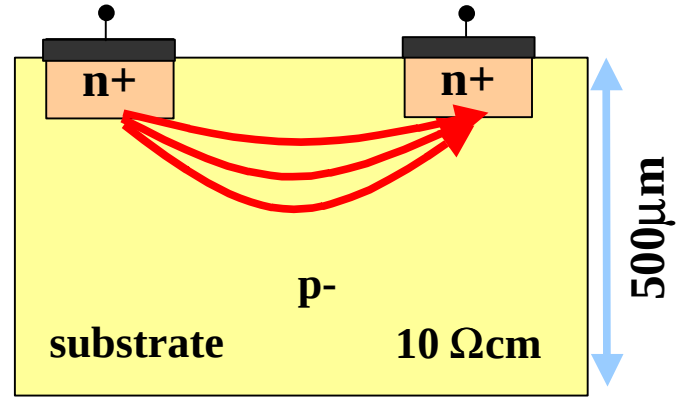
IMEC - DESICS - MIRA

Kapeldreef 75, B-3001 Leuven, Belgium

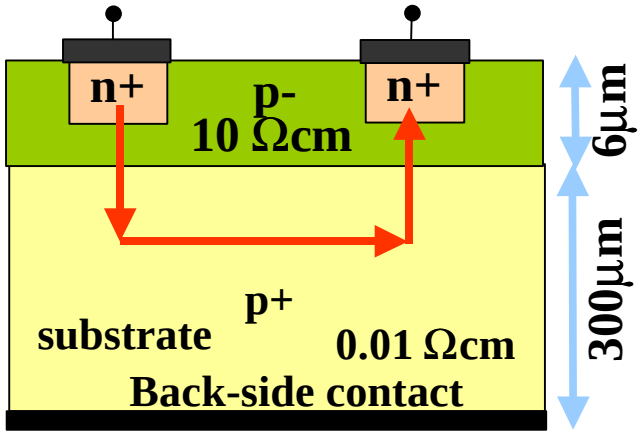
AIM

To simulate the substrate noise generation from large digital circuits on the substrate fast and accurately during gate-level VHDL simulations.

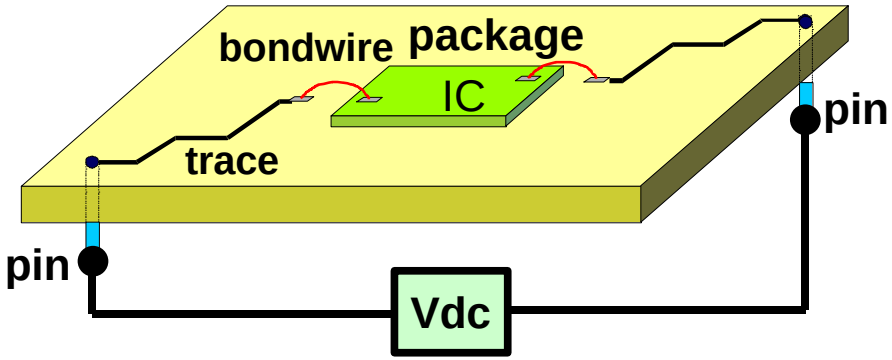
Substrate types and packages shape the noise.

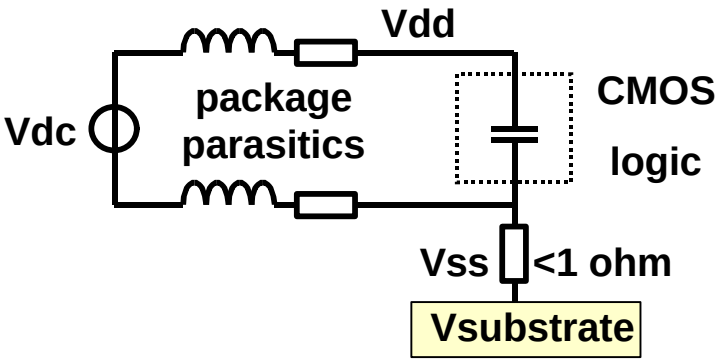


UNIFORMLY DOPED SUBSTRATE



EPI-TYPE HEAVILY DOPED SUBSTRATE





AIM: To analyze the substrate noise generation at gate level

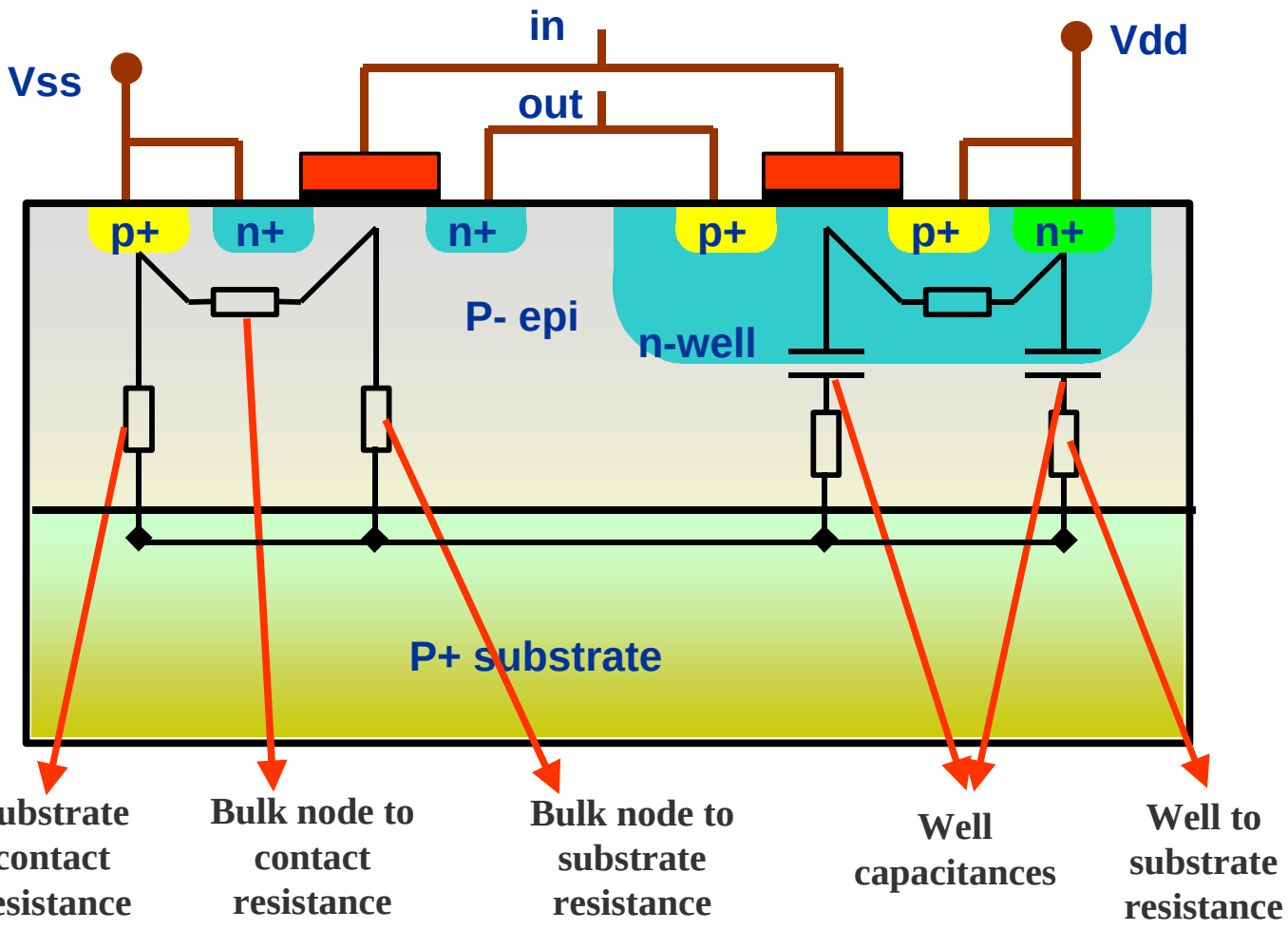
EXISTING APPROACHES

- Performed after layout
- Accurate, but slow
- Need for a new testbench
- SPICE simulations after extraction

OUR APPROACH: Substrate Waveform ANalysis

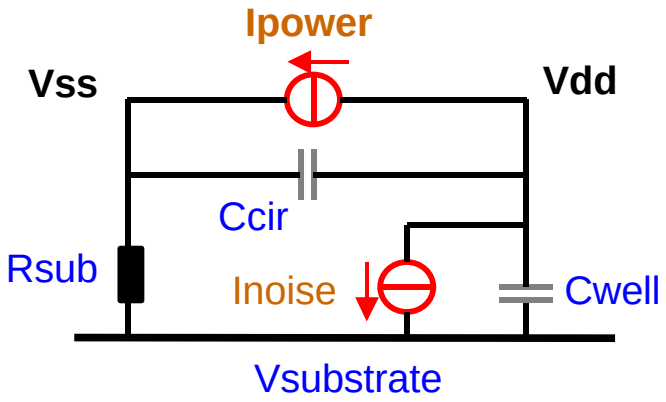
- Performed during the gate level
- Accurate and fast
- Same testbench used for functional verification
- Event-driven simulation

Gate substrate model in an epi-type CMOS process

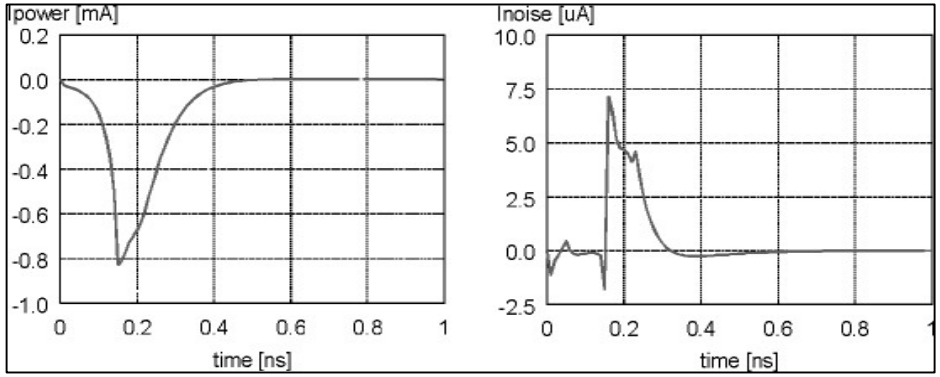


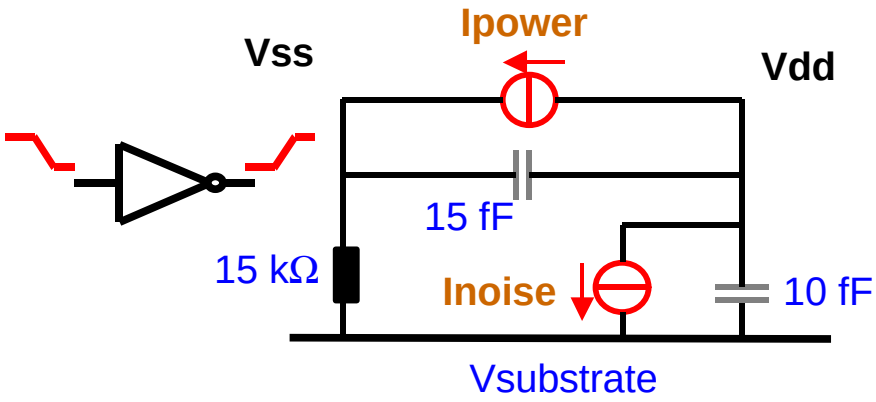
SUBMACRO library characterization

- **In gate substrate macro model**
  - supply current
  - power-ground circuit capacitance
  - substrate current injection current
  - substrate contact resistance
  - well capacitance



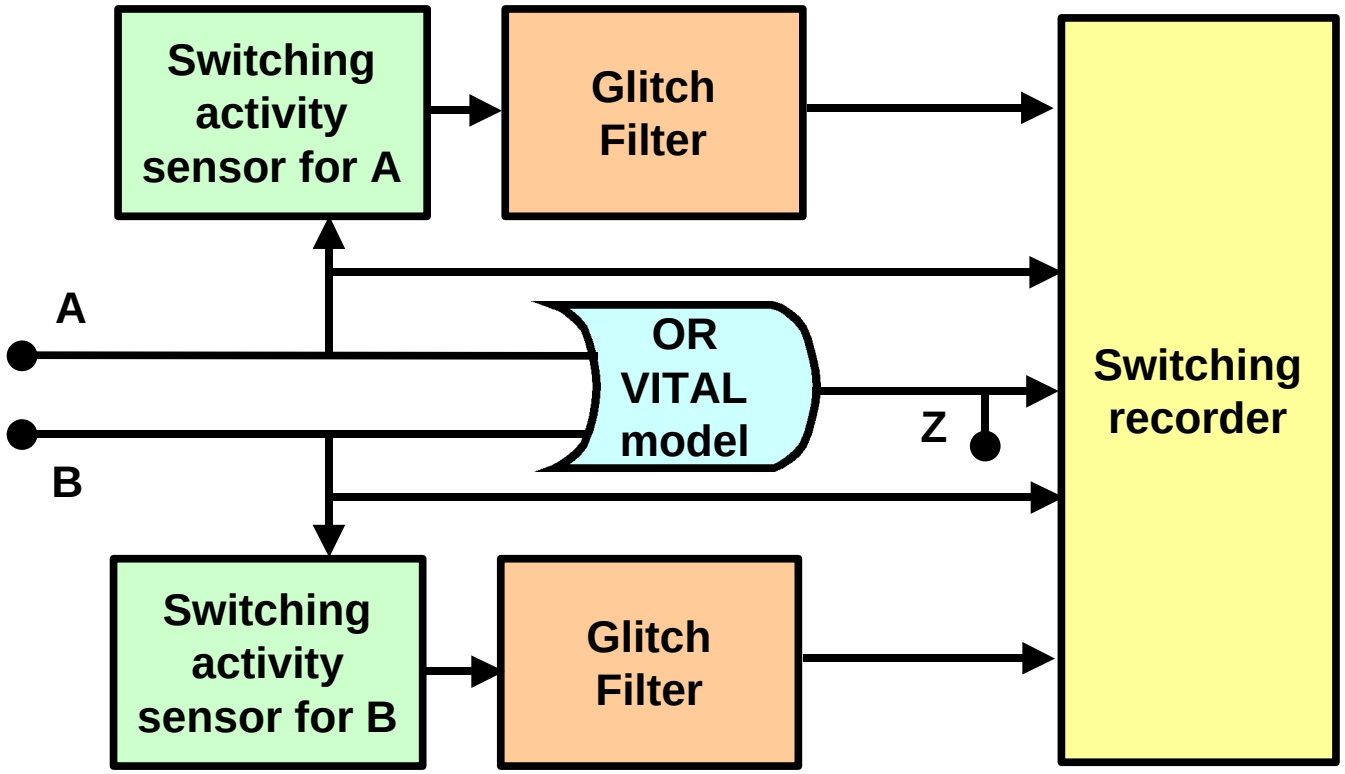
- **Current waveforms**



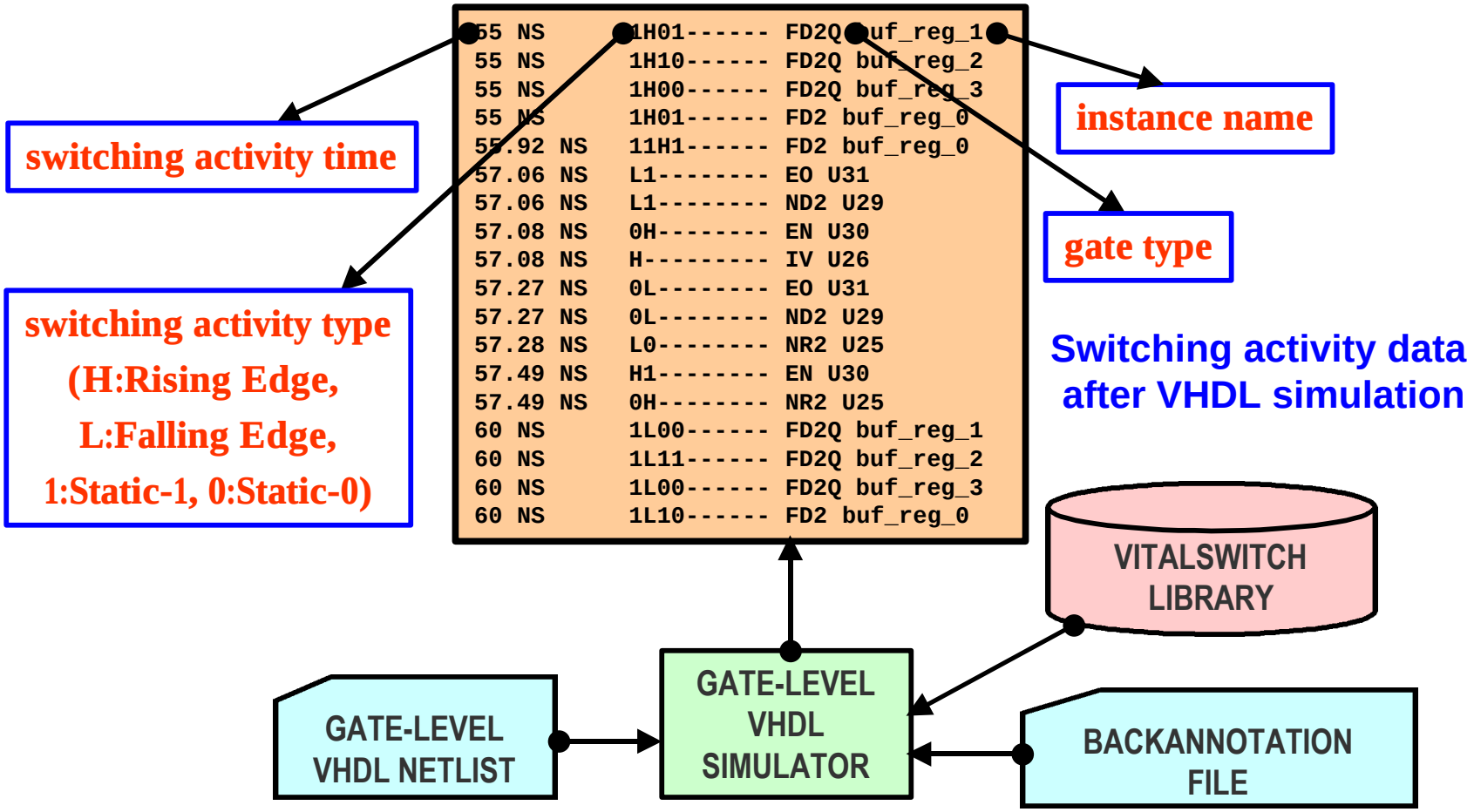


VITALSWITCH library characterization

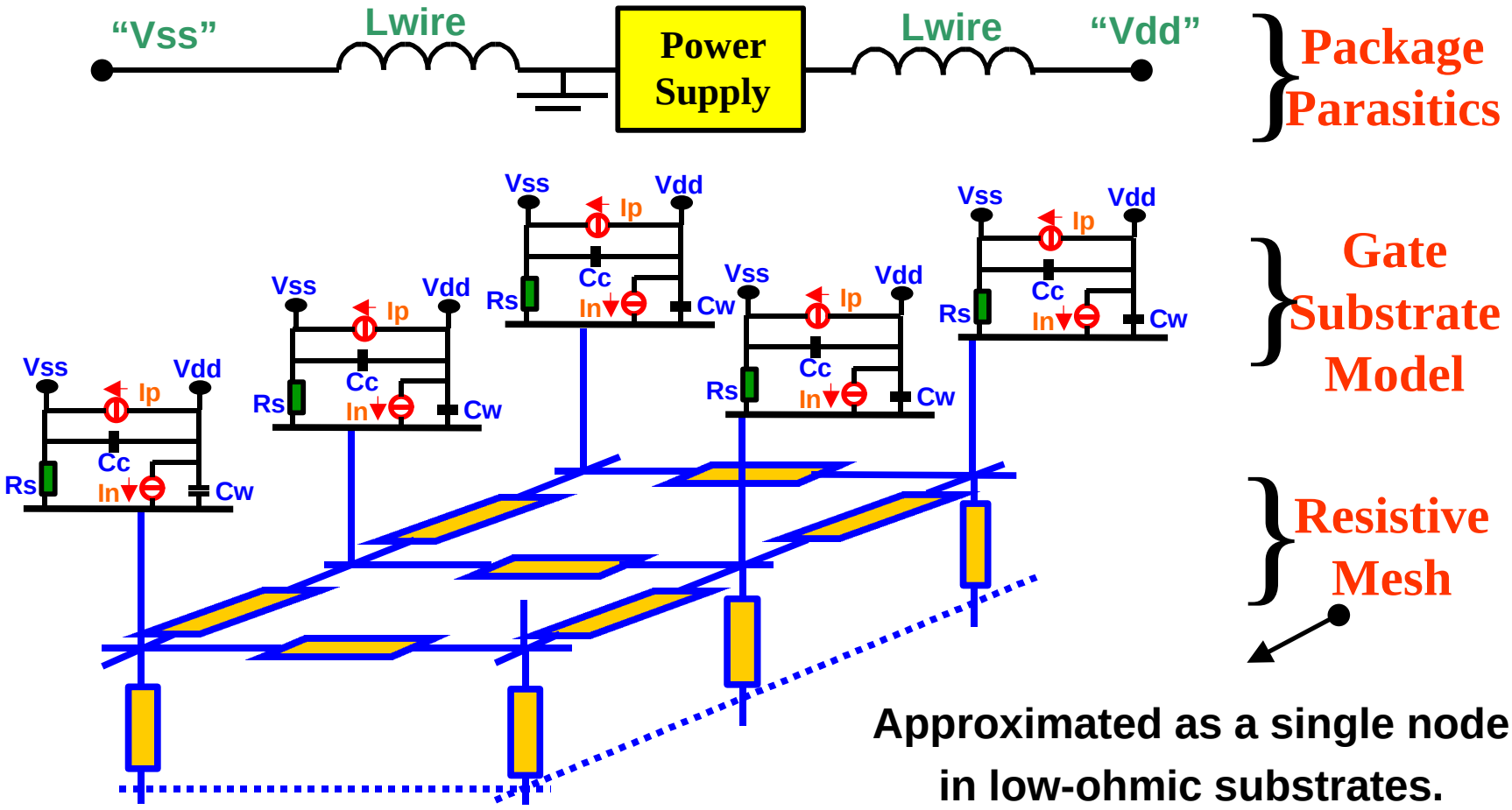
VITAL models are extended to record input switching activities.



Gate-Level VHDL simulation with VITALSWITCH records the switching activities.

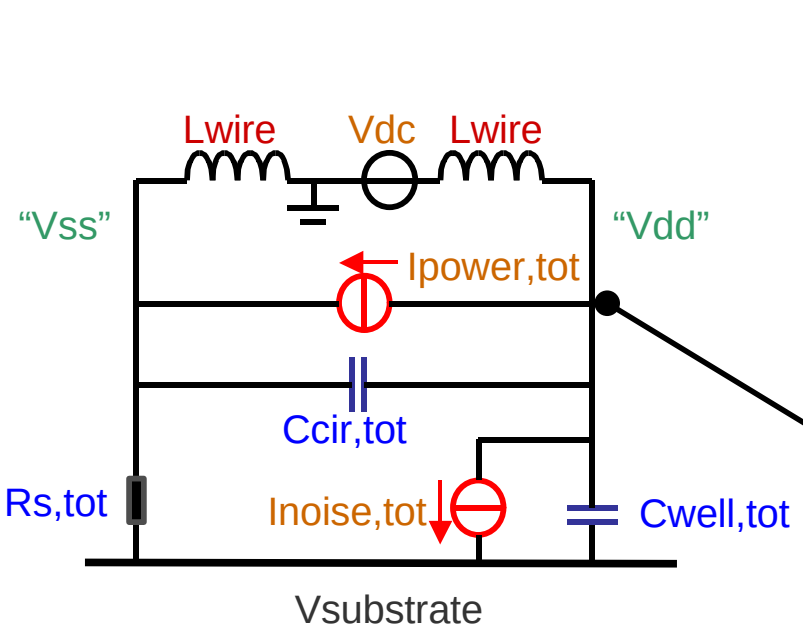


System substrate macro model extraction

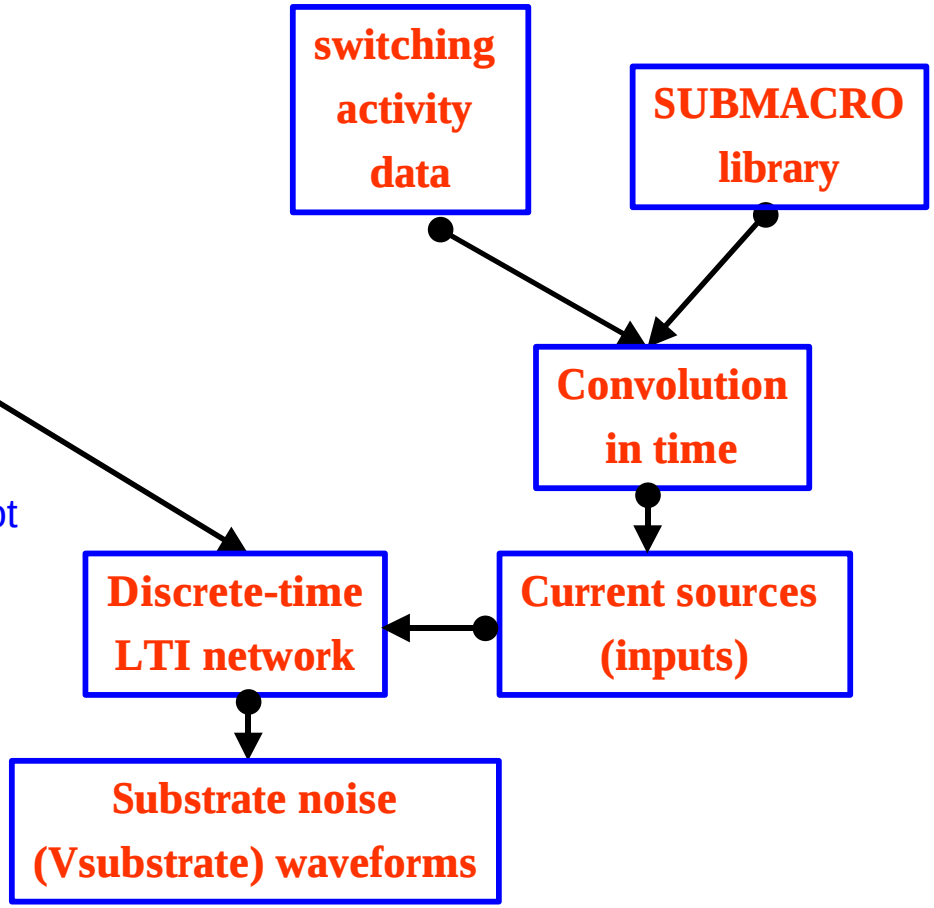


Approximated as a single node in low-ohmic substrates.

Switching activities are convolved with SUBMACRO library to simulate the extracted circuit.



Extracted system substrate model for low-ohmic epi-type substrate

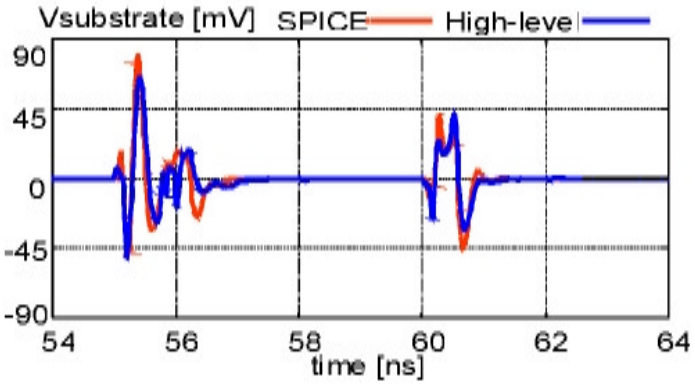


Substrate Waveform ANalysis Flow

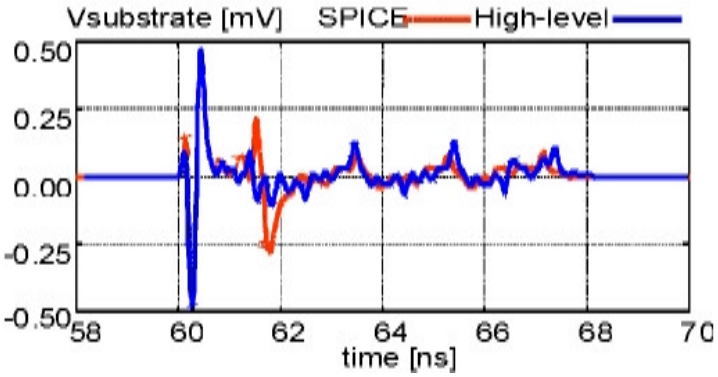
- **Library characterization**
  - Gate substrate macro model library (SUBMACRO)
  - VHDL library for switching event recording (VITALSWITCH)
- **VHDL gate-level simulation to record switch activities**
- **Extract system substrate macro model**
- **Simulate system substrate macro model**

Speed and accuracy compared to SPICE

With 2nH + 0.5Ω



No Package parasitics



- 4-bit counter (34 gates)
- 13 switching events after rise edge of clock (55ns)
- 2.4 % error between RMS substrate voltages
- 490x time speedup

- 16-bit multiplier with two counters (1K gates)
- 170 switching events after rise edge of clock (60ns)
- 5.4 % error between RMS substrate voltages
- 2522x time speedup

=> Even, for a 80Kgate multi-channel select filter, it takes 13 minutes to simulate for 50 clock cycles.

2. Evaluation of the substrate noise effect on analog circuits in mixed-signal designs

Yann Zinzius, Erik Lauwers, Georges Gielen, Willy Sansen

K. U. Leuven - ESAT - MICAS

Kardinaal Mercierlaan 94, B-3001 Heverlee, Belgium

AIM

- **Increase of the design complexity**

  => interest to analyze impact of digital noise on analog design

  => predict performances degradation

- **Tools are available (Layin, Space, SCA)**

  problem : require large memory and CPU time

  solution : provide a simple model to predict noise influence on analog design

Digital Noise and Analog Design

- **Impact on analog design**
  - **Threshold voltage of the MOS transistor**

$$V_t = V_{t0} + g \cdot \left(\sqrt{2 \cdot f_f + V_{SB}} - \sqrt{2 \cdot f_f} \right)$$

$$\frac{gmb}{gm} = \frac{g}{2 \cdot \sqrt{2 \cdot f_f + V_{SB}}} = c$$

$$I_D = \frac{KP}{2} \cdot (V_{GS} - V_t)^2$$

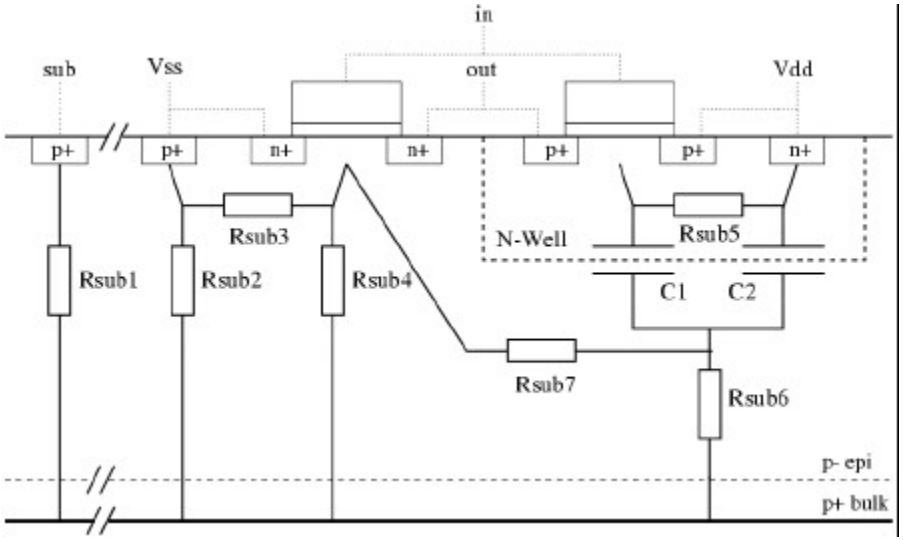
  - **Capacitive coupling between substrate and devices (junction or coupling capacitances)**

- **Sensitive analog part**
  - **Passive devices capacitively coupled with the substrate**
  - **Low signal input stage**
  - **Single ended <-> differential**

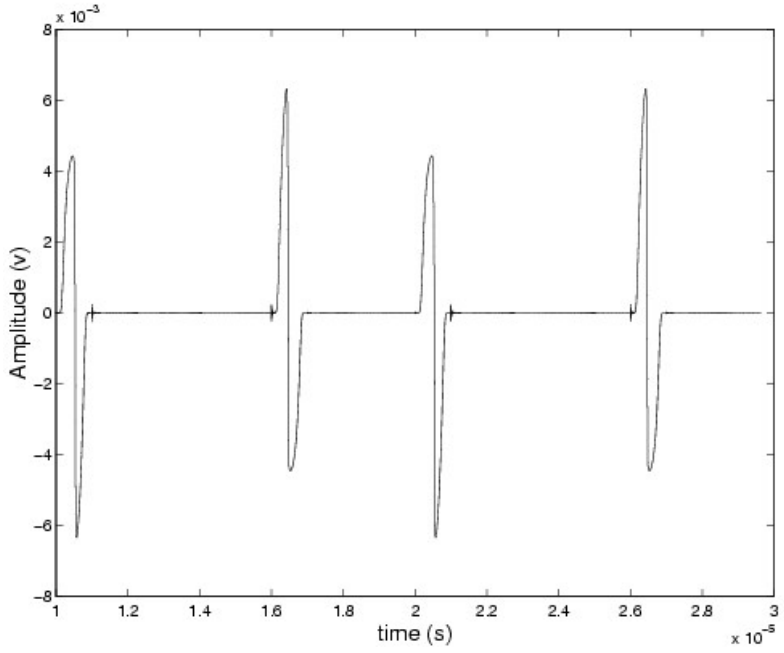
- **Protection techniques**
  - **Common mode noise => fully differential design**
  - **Decoupling capacitance**
  - **Guard ring**
  - **Phase shifting between digital clock and analog sampling**

Substrate Model

- **Substrate model extracted from a layout for an inverter**
  - **Technology mietec 0.35 μm**
  - **Epitaxial layer ($\rho \cong 10 - 13\ \Omega.cm$)**
  - **Nwell ($\rho \cong 13\ \Omega.cm$)**
- **Include :**
  - **Bulk Resistance ($Rsub_i$)**
  - **Well Capacitance (C_i)**
- **Order of magnitude :**
  - **Rsub5 ≅ 100 Ω**
  - **Rsub3 ≅ 100 kΩ**
  - **Rsub2 ≅ 10 kΩ**
  - **Rsub4 ≅ 10 kΩ**



Simulation Setup (1)

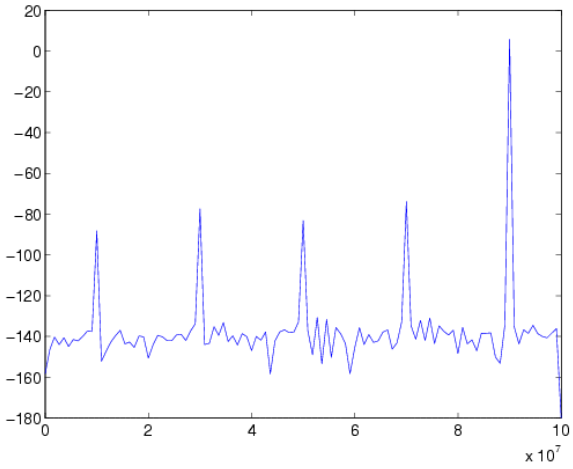


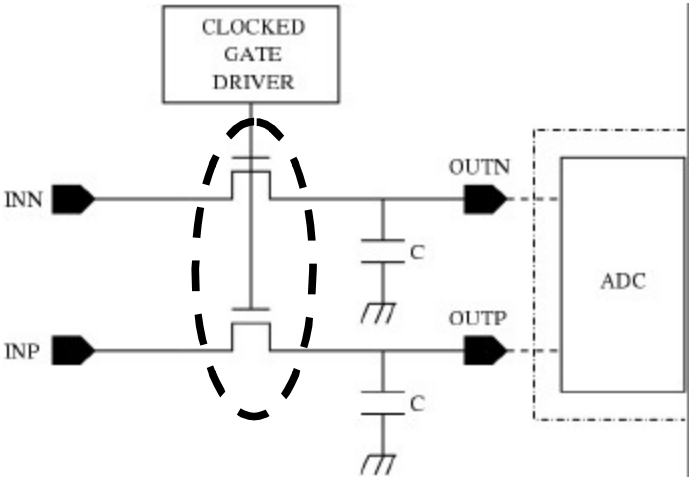
- **Reduced substrate model**
  - **Bulk resistance**
  - **Power supply inductance**
- **Junction capacitance already implemented in SPICE model**
- **Noise source model based on simulation results**
- **Nominal bulk resistance values obtained from transistor layout extraction**

Simulation Setup (2)

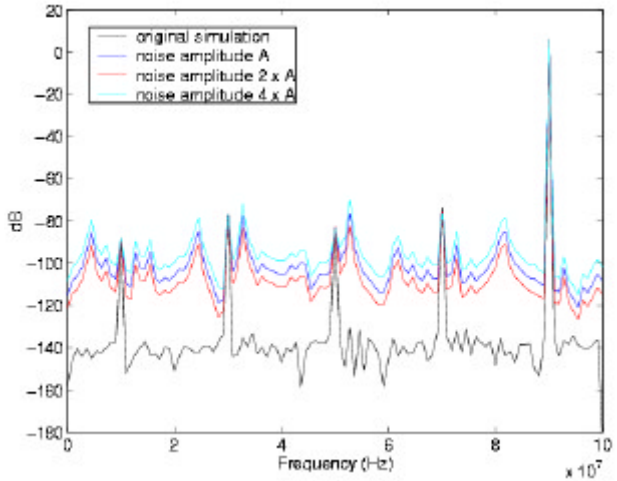
- Simulation of a high-resolution Sample and Hold.
- Structure partially differential

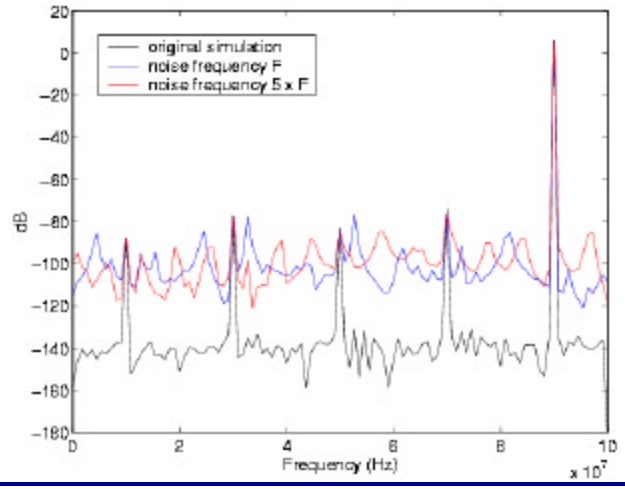
  => addition of a mismatch model
- Technology Mietec 0.35 μm CMOS
- Sinusoidal input at 90 MHz.
- Transient simulation with Fourier analysis.





Simulations Results (1)

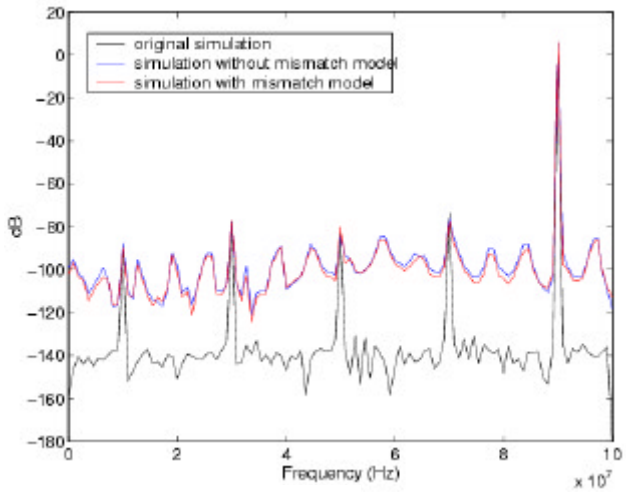


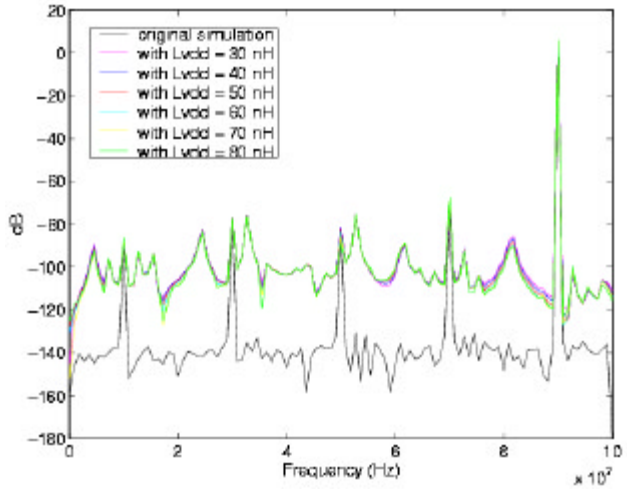


- **Amplitude variation**
  - **Double of the noise amplitude => Output signal increase of 10 dB**
  - **Exponential relation between noise amplitude and output signal for a given frequency**
- **Frequency variation**
  - **Affects the output signal in non predictable way**
  - **Noise amplitude not affected**

Simulations Results (2)

- **Simulation with and without mismatch model added**
  - **Low sensitivity of the design to mismatch**
  - **No fully differential technology**
- **Variation of the bondwire inductance**
  - **Low sensitivity of our design**





Simulation Time

- Extraction of an analog design with the existing tool requires some hour (if possible !!!)
- CPU time needed for Sample and Hold simulation => tens of minutes (on H.P. C360 mono-processor)
- Simulation presented => 2X longer than simulation without substrate model added

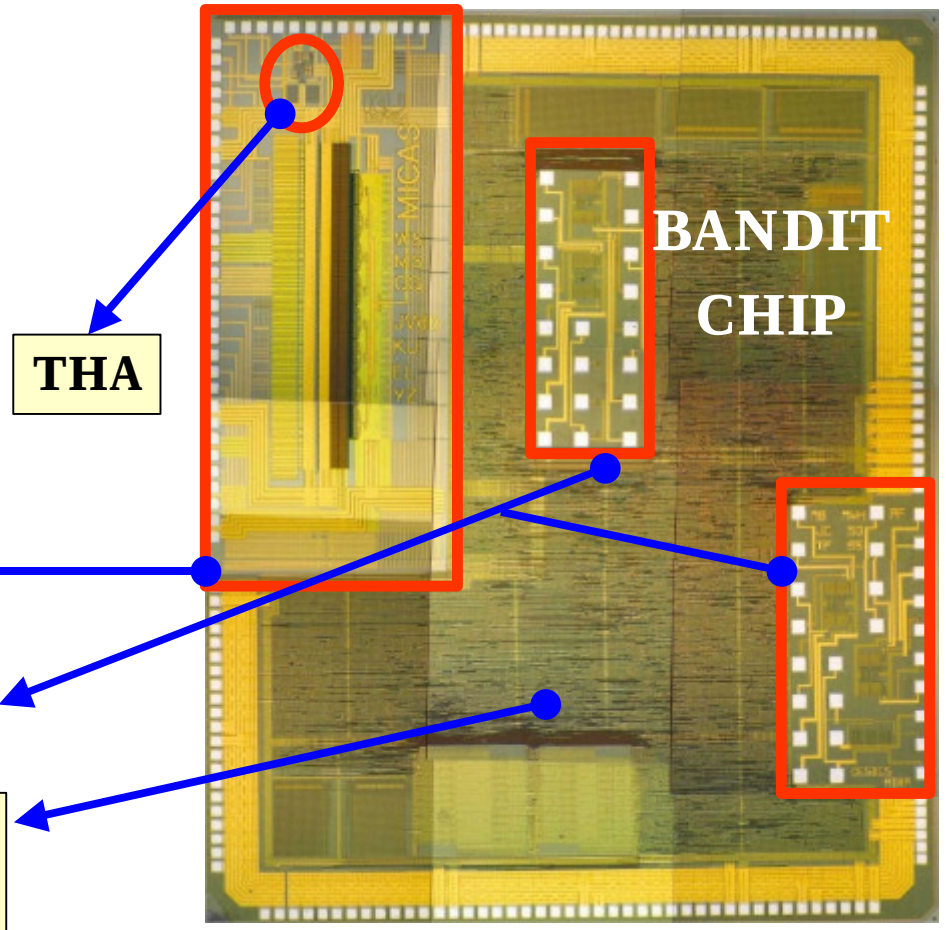
Conclusions

- The presented substrate noise coupling analysis takes into account noise generation by large digital circuits and impact on ADC performance.
- The presented gate-level simulation of substrate noise generation is fast and accurate in comparison with SPICE simulations.
- The presented technique for the impact of substrate noise on analog circuits:
  - fast solution to estimate substrate noise effect on analog topology
  - easy to implement in SPICE netlist
- Future work: The presented technique will be compared with measurement results (Bandit chip).

Future Work: Verification of the methodology with measurements

WLAN TX/RX OFDM-MODEM INCLUDING
IQ MODULATOR - IQ DEMODULATOR,
ANALOG-TO-DIGITAL CONVERTER (ADC)
WITH TRACK-AND-HOLD AMPLIFIER (THA),
ON-CHIP NOISE SENSORS

220K GATE EQUIVALENT DIGITAL AREA,
176 IO PINS (44 Analog, 131 Digital, 1 N/A)
60 MHz-20 MHz GATED CLOCKS



Project partners

The research is sponsored by ESPRIT BANDIT project.

KATHOLIEKE UNIVERSITEIT
LEUVEN

ERICSSON