

High-Level Simulation of Substrate Noise Generation from Large Digital Circuits with Multiple Supplies

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Abstract

Substrate noise generated by large digital circuits degrades the performance of analog circuits sharing the same substrate. Existing approaches usually extract the model of the substrate from the layout information and then simulate the extracted transistor-level netlist with this substrate model using a transistor-level simulator. For large digital circuits, the substrate simulation is however not feasible with a transistor-level simulator. In our previous work, it has been demonstrated that efficient and accurate simulation of substrate noise generation at gate-level is feasible. In this paper several important extensions to our previous work are introduced: modeling of IO cells, modeling of input transition time and load dependency and the extraction methodology of an equivalent substrate model within multiple supply domains. Experimental results show an improved accuracy (6.3% error on RMS substrate voltage with respect to a full SPICE level simulation) with these extensions, while maintaining a large speedup with respect to SPICE simulations.

1. Introduction

There is a trend in the semiconductor industry towards single-chip integration of more complex systems, higher speeds and lower supply voltages where signal-integrity analysis becomes a challenging task. Substrate noise coupling is a vital factor in the signal integrity analysis.

Recently, substrate noise coupling research has concentrated mostly on the propagation of the substrate noise [1][2]. All these techniques model the substrate as a network of resistors and capacitors attached to the nodes of the transistor-level netlist. The simulation of the transistor-level netlist with its substrate model requires many computer resources and is time consuming. Another disadvantage is that the approaches start from the layout of the circuit. However, there is a need for an analysis methodology during the design phase of the large digital systems, e.g. during gate level design. There are a few publications

on the gate-level simulation of noise generation from a large digital circuit. In [3][4], methodologies are presented to simulate the substrate noise generation using an event-driven simulator. The mathematical functions to formulate the noise for each switching activity are rather simple. Methodologies that make use of real substrate noise waveforms for each standard cell are presented in [5][6]. In [6] the noise coupling from the supply lines and the transistors is modeled for each standard cell.

In this paper, several important extensions to the fast and accurate simulation methodology of [6] are presented, such as the modeling of IO cells with multiple supplies, the modeling of input transition time and load dependency, and multiple supply domains. We will show that these extensions significantly increase the accuracy of the substrate noise analysis without compromising the speedup.

2. Overview of gate-level substrate noise analysis and macro cell modeling

For each core cell and IO cell in the standard cell library, we develop a substrate macro model containing supply current sources and a switching noise (noise through the bulk node) current source for each possible input and state combination, taking input transition time and the load dependency into account. This standard cell characterization is performed once for every technology. The results are stored in the SUBMACRO library, which contains the substrate model of each cell. Next, we perform a gate-level simulation of the digital system to store all the switching activities using the SWITCHVHDL library. Then we extract the equivalent substrate model of the total digital system at chip level considering multiple supply domains with their corresponding package parasitics. With this equivalent model, the total substrate voltage is computed. An overview of this simulation methodology is shown in Figure 1. The resulting substrate noise source can then be connected to the substrate node of a sensitive circuit to see the impact of the noise.

The substrate model for an inverter is shown in Figure 2-a. The substrate types that we consider here are low-ohmic substrates (bulk resistivity of $10 \text{ m}\Omega\text{cm}$), which have a better latch-up immunity as compared to high-ohmic substrates. For low-ohmic substrates, a single electrical node can approximate the entire substrate. The horizontal resistances between the standard-cells are larger than vertical resistances along the p-epi layer as the thickness of the p-epi layer is small ($\sim 4\mu\text{m}$). Therefore, we can represent every standard cell in a π -circuit model, which simplifies the model reduction at chip level, and we can neglect horizontal resistive paths between standard cells. The element values are calculated using empirical formulas, taking into account geometry information of the substrate contacts and nwells [7]. Experimental verification of this model was presented in [8]. This model is used as reference for the verification of our high-level simulation methodology in Section 5.

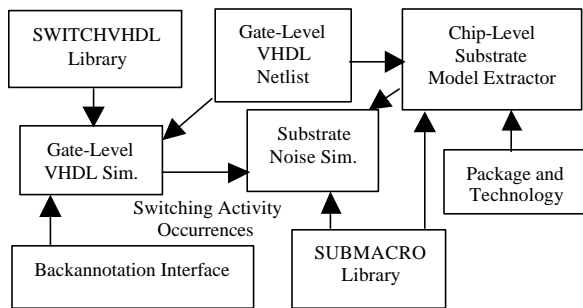


Figure 1 Simulation methodology flow

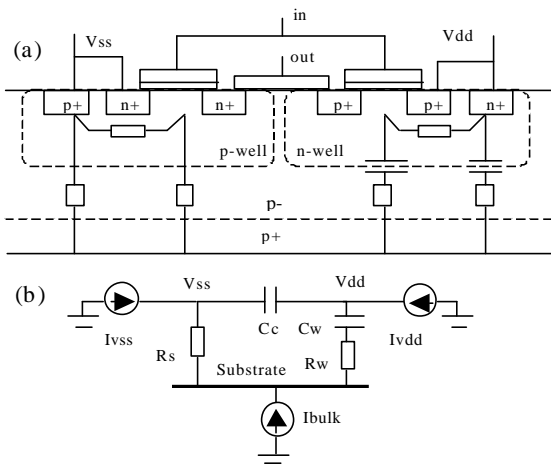


Figure 2 (a) Spice model for an inverter (b) Macro cell for a standard core cell

The macro cell models (also for a cell with multiple supplies) contain two types of current sources: one, which models the coupling from the switching MOSFETs

(I_{bulk}), and two sources, which model the power supply current (I_{vss} , I_{vdd}). The current generated by the switching gate is injected into the substrate and flows back to the AC ground via the substrate. The impedance between the AC ground and the substrate can be modeled by a parallel combination of a resistance and a series connection of a capacitance and a resistance. The macro cell model is shown in Figure 2-b. The current source waveforms in this model are derived in such a way that the macro cell model produce the same substrate voltage as the transistor-level model shown in Figure 2-a. This is a good approximation up to several GHz, as shown in [6].

3. Multiple supply domains

3.1. Modeling of IO cells

In [6] no models for IO cells were included. However, experimental results have shown that switching IO buffers contribute up to 30% of the total substrate noise power generation. A typical IO cell has two power supplies. One (v_{dde} , v_{sse}) is used for the last output stage of cascaded buffers while the other supply (v_{dd} , v_{ss}) is used for the remaining buffers and circuitry. Such a separation in the supplies is necessary as the last output stage of the IO cell is usually noisy and the ground of this supply (v_{sse}) is not connected to the substrate, whereas the core supply ground (v_{ss}) is mostly connected to the substrate. For the cells, which have multiple supplies, circuit capacitances are extracted between different supply pairs so that the coupling between the supply domains is included in the model. This is equivalent to an impedance matrix extraction for an N-port device. The rest of the parameters are computed in a similar way as for a standard core cell with a single power supply. In Figure 3, an example is shown of the macro model of an IO cell with multiple supplies.

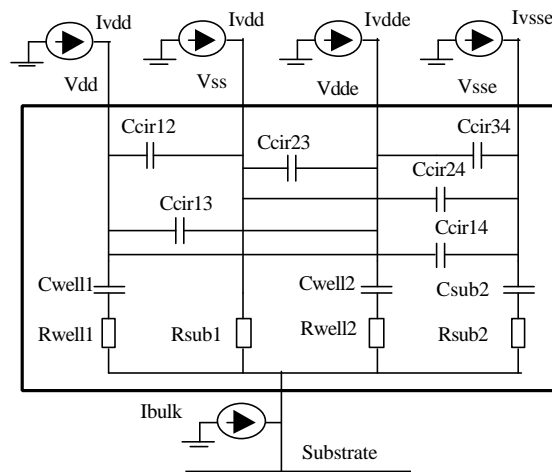


Figure 3 Macro cell model for an IO cell

Notice the presence of capacitor Csub2 because the ground is not connected to the substrate for the vdde-vsse supply domain. The validity of the IO macro cell model has been verified and compared to a full SPICE simulation of the extracted netlist of the IO cell by means of the tool SubstrateStorm[9], as depicted in Figure 4.

3.2. Equivalent System Substrate Model for Multiple Supply Domains

Generation of an equivalent system substrate model is necessary for the substrate noise simulation with the extracted switching activities.

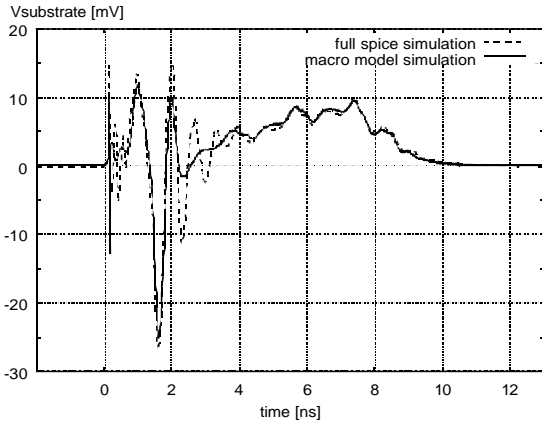


Figure 4 Substrate voltages from an IO cell for the macro cell model and SPICE model

The macro cell models are combined together within their corresponding supply domain, as the substrate node is common for each macro cell model on epi-type substrates. Following expressions are used for model reduction of a network in supply domain i :

$$R_{sub}(i) = \left(\sum_{\substack{j=\text{all gates} \\ \text{within domain } -i}} \frac{1}{R_{sub}(i, j)} \right)^{-1}$$

$$C_{well}(i), cir(i) = \sum_{\substack{j=\text{all gates} \\ \text{within domain } -i}} C_{well}(i, j), cir(i, j)$$

$$I_{bulk}(i, t) = \sum_{\substack{j=\text{switching events} \\ \text{within domain } -i}} I_{bulk}(t - \beta \cdot t[i, j]) \times \frac{1}{\beta}$$

$$I_{power}(i, t) = \sum_{\substack{j=\text{switching events} \\ \text{within domain } -i}} I_{power}(t - \beta \cdot t[i, j]) \times \frac{1}{\beta}$$

In the above expressions β is a factor used for the time and the amplitude scaling, which models input transition time dependency of the current waveform for the macro cell model (see Section 4). After the model reduction of the cells, package parasitics are attached to each supply

domain. An example of a chip with three supplies is shown in Figure 5. The chip consists of core cells grouped into two supply domains and IO cells with two supplies, where one of the supplies is a core supply and the other one is an additional supply specific for IO cells (vdde, vsse). The network itself with all lumped elements and independent current sources is represented as an s-domain transfer function with multiple inputs. This transfer function is then transformed into a z-domain transfer function to perform the simulation with difference equations to increase the simulation speed. The supply currents and the bulk current in the SUBMACRO library are generated for any input switching activity. However, as will be discussed in Section 4, input transition time and load have an impact on those currents.

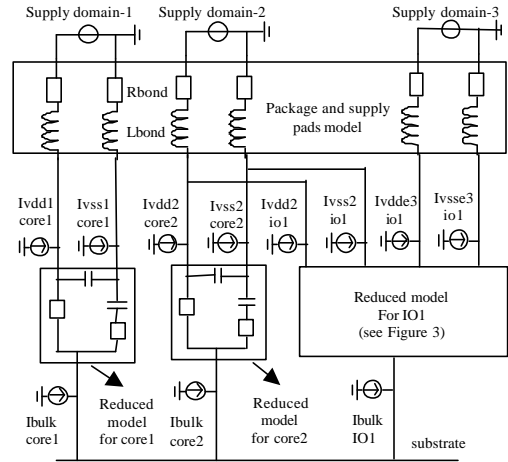


Figure 5 Equivalent chip substrate model

4. Modeling of Input Transition Time and The Load on Macro Cell Models

The load as well as the input transition (rise and fall) time has an important influence on currents flowing within a gate, supply rails and the load itself during the switching event. For an accurate simulation of the substrate noise, it is therefore important to model the input transition time and the load within the macro cell models.

In the VHDL simulation all input switching activity is recorded, also for the inputs that do not cause output switching. However, load dependency of the supply currents and the bulk current becomes important, only when the output is switching. An example of load dependency for a NAND2 gate is shown in Figure 6-a. As the load increases, the supply current pulsewidth of the macro cell model increases without a change in the amplitude. For the bulk current, the effect is seen as a decrease in the amplitude without a change in the pulsewidth.

On the other hand, input transition time dependency is always important, whether the output is switching or not. The pulsewidth of the current waveforms increases and the amplitude decreases with an increase in the input transition time. An example is shown for the input transition time dependency for an NAND2 gate in Figure 6-b.

The SUBMACRO library is implemented as a look-up table, which contains the waveforms for combinations of load values (Cl) and different switching activity types (Swi). Those waveforms are extracted for a given constant input transition time. When a switching activity occurs for a gate with a different input transition time, the amplitude and the pulsewidth of the waveform are modified. This modification of the waveform is shown in Figure 7.

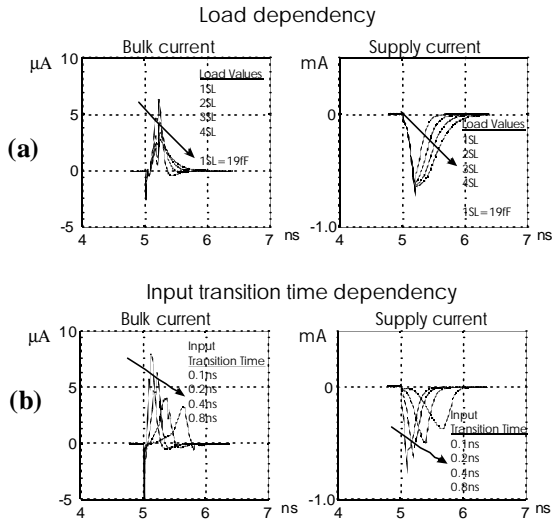


Figure 6 (a) Load and (b) input transition time dependency for an NAND2 gate

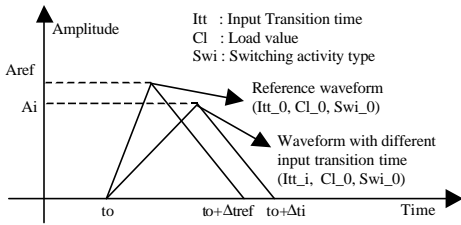


Figure 7 Input transition time effect on current

The change in the pulsewidth and the amplitude of the waveform due to the input transition time is as follows:

$$\Delta t_i = \Delta t_{ref} + I_{tt_i} - I_{tt_0} \quad A_i = A_{ref} \times \frac{\Delta t_{ref}}{\Delta t_i}$$

$$b = \frac{\Delta t_i}{\Delta t_{ref}} \quad : \text{Amplitude - time scaling factor}$$

Using the β factor, the expansion/compaction in time and decrease/increase in the amplitude are computed after the current waveform is fetched from the look-up table with its corresponding load and switching activity type. Because of load and input transition time dependency and multiple supply regions, additional attributes are necessary for each instance in the switching activity file generated by the gate-level VHDL simulation. These are load, input transition time, supply domain, switching activity type, gate type, time of switching, and a flag indicating an output switching. The input transition time for each port and the loads are computed with the use of the fanout and the net loads from backannotation.

5. Experimental Results

In this section, the comparison between high-level (SWAN) and SPICE simulations will be shown for a test circuit, count8disp (8-bit counter with a 7-segment display). This circuit, shown in Figure 8, is simulated for 20 clock cycles using two experiment groups (A and B). Each of the SWAN simulations within a group is compared with the corresponding full SPICE level simulation used as a reference such that A-n and B-n is compared with A-ref and B-ref respectively. For each scenario within a group, simulation time, RMS value and maximum peak-to-peak value of the substrate voltage are recorded to derive accuracy and the speedup figures (see Table 1).

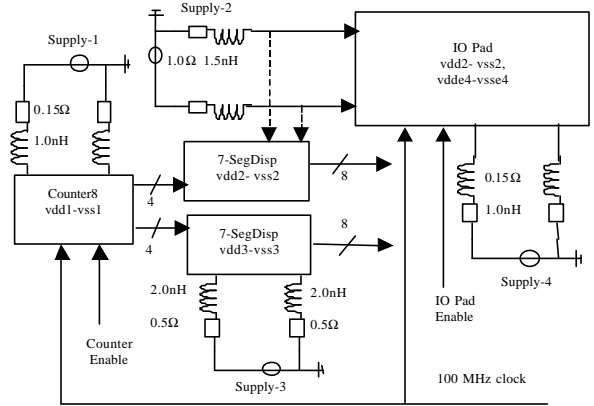


Figure 8 Architecture of count8disp

For experiment group-A, the comparison shows that the accuracy increases whenever the extensions such as input transition time, load dependency, and multiple supply domains are added into the SWAN simulation methodology. The error on the RMS substrate voltage is reduced from 27.3% to 17.4% when only the load and input transition time dependency are included. Multiple power domains should not be neglected since each power domain has its own specific ringing frequency, which is visible in the

generated substrate noise spectrum. The overall combination of load and input transition time dependency together with multiple supplies gives the maximum accuracy.

For experiment group-B, a single output pad is added into the circuitry in order to make a comparison between SWAN simulation with all the extensions and the full SPICE simulation (see Table 1). The comparison between A-ref and B-ref shows that the IO pad is responsible for 30% of the total substrate noise power generation.

Table 2 summarizes the simulation details and times for count8disp together with two other examples, mult8 (8-bit multiplier circuit [6]) and Robo4 (multi-rate channel selection filter). For larger circuits, the speedup with respect to full SPICE level simulations becomes higher. For very complex digital circuit, like the 80Kgate circuit Robo4, SPICE simulations are no longer feasible.

Table 1 Results for count8disp

Test	Description				
A-ref	Spice simulation of the circuit in Figure 8 (without IO pad).				
A-1	SWAN (without no extensions)				
A-2	SWAN + inp. trans. time / load				
A-3	SWAN + multiple supplies				
A-4	SWAN + multiple supplies + inp. trans. time/load				
B-ref	Spice simulation of the circuit in Figure 8 (with IO pad).				
B-1	SWAN + multiple supplies + inp. trans. time/load + IO model				
Test	V _{sub,RMS} [mV]	V _{sub,PPmax} [mV]	ErrRMS [%]	ErrPPm [%]	SimTime [s]
A-ref	4.852	87.70	0	0	3572
A-1	3.525	56.62	27.3	35.4	27
A-2	4.006	79.42	17.4	9.4	30
A-3	3.858	54.54	20.5	26.4	38
A-4	4.554	93.48	6.1	6.1	48
B-ref	6.922	103.18	0	0	14940
B-1	7.361	119.88	6.3	16.2	70

Table 2 Results for the test circuits

	Count8disp	Mult8*	Robo4*
Core gate equiv. area	278	994	81298
Total gate equiv. area	728	994	89132
Clock Period / Cycles	10ns / 20	25ns / 200	20ns / 50
# Switching Activities	5056	63106	76205
Model Extract Time	0.10 sec	0.13 sec	6.02 sec
Spice Sim. Time	14940 sec	37 hours	--
VHDL Sim. Time	38.64 sec	30.12 sec	11:43 min
Substrate Sim. Time	31.29 sec	18.67 sec	41.14 sec
High-Level Sim. Time	69.93 sec	48.79 sec	12:24 min
Speed-Up	x213	x2730	--

*) simulation without load and input transition time dependency

6. Conclusion

The traditional approach of using a transistor-level simulator to predict the amount of substrate noise generation is not feasible for large digital systems. In this paper, a methodology (SWAN) has been presented to efficiently simulate the substrate noise waveforms of complex digital systems, including several important extensions. First, a

substrate noise macro model for IO buffers has been presented that can easily be integrated in the high-level simulation methodology. Since switching-noise from IO buffers can contribute up to 30% of the total noise generation, these models need to be included in a high-level simulation. Next, multiple supply domains are included, which is both important for accurate simulation of the noise generation (especially because ringing on each supply will couple to the substrate) and for analyzing which supply domain is causing most substrate noise. Finally, the output load and input transition time dependency has been implemented in SWAN. The improved high-level substrate noise simulation methodology (SWAN) can simulate the substrate noise voltage within %6.3 of a full SPICE level simulation, with a speedup of 213 times.

References

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